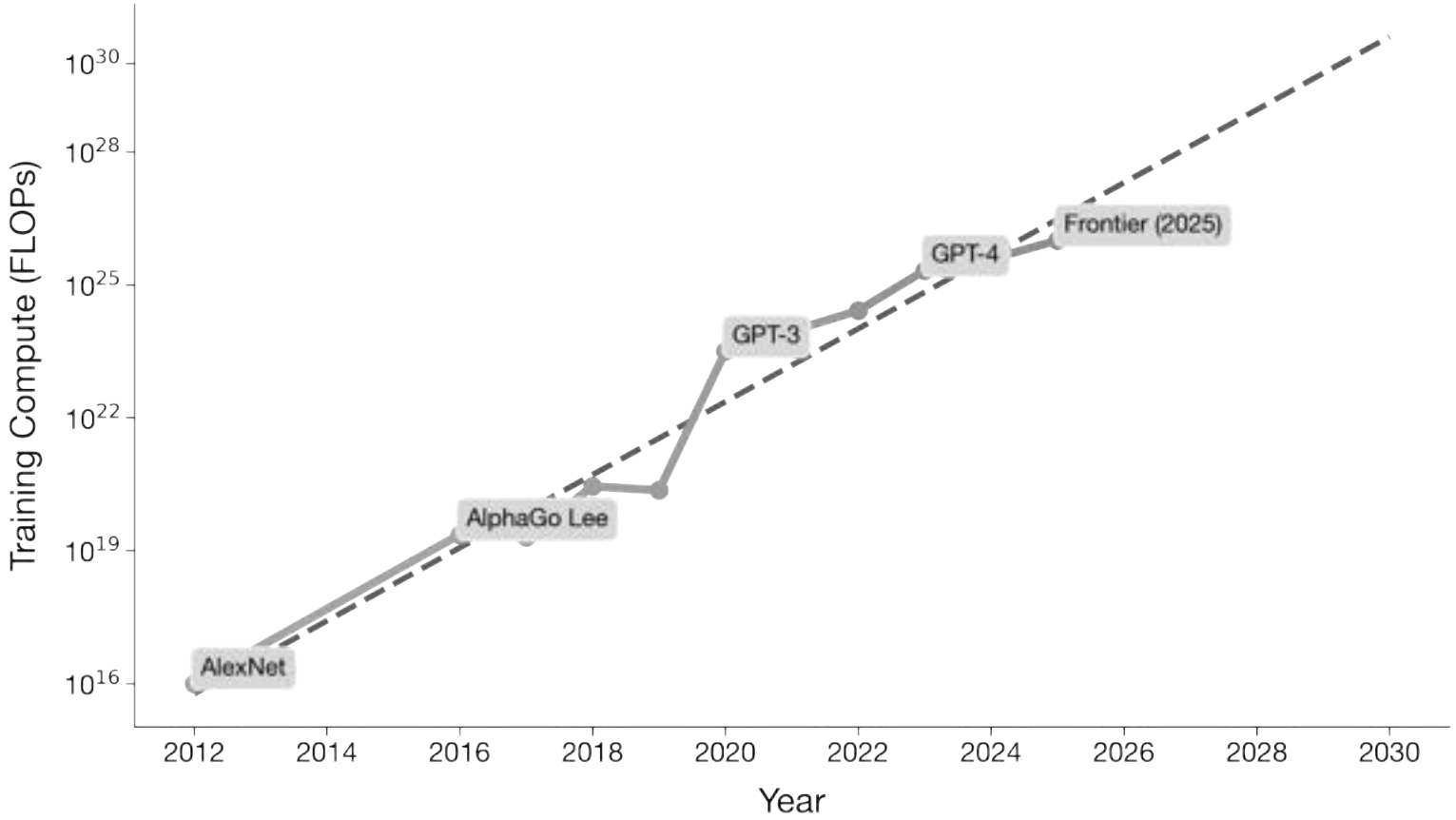
Scaling AI with Photonic Interconnects: Integration and Manufacturability

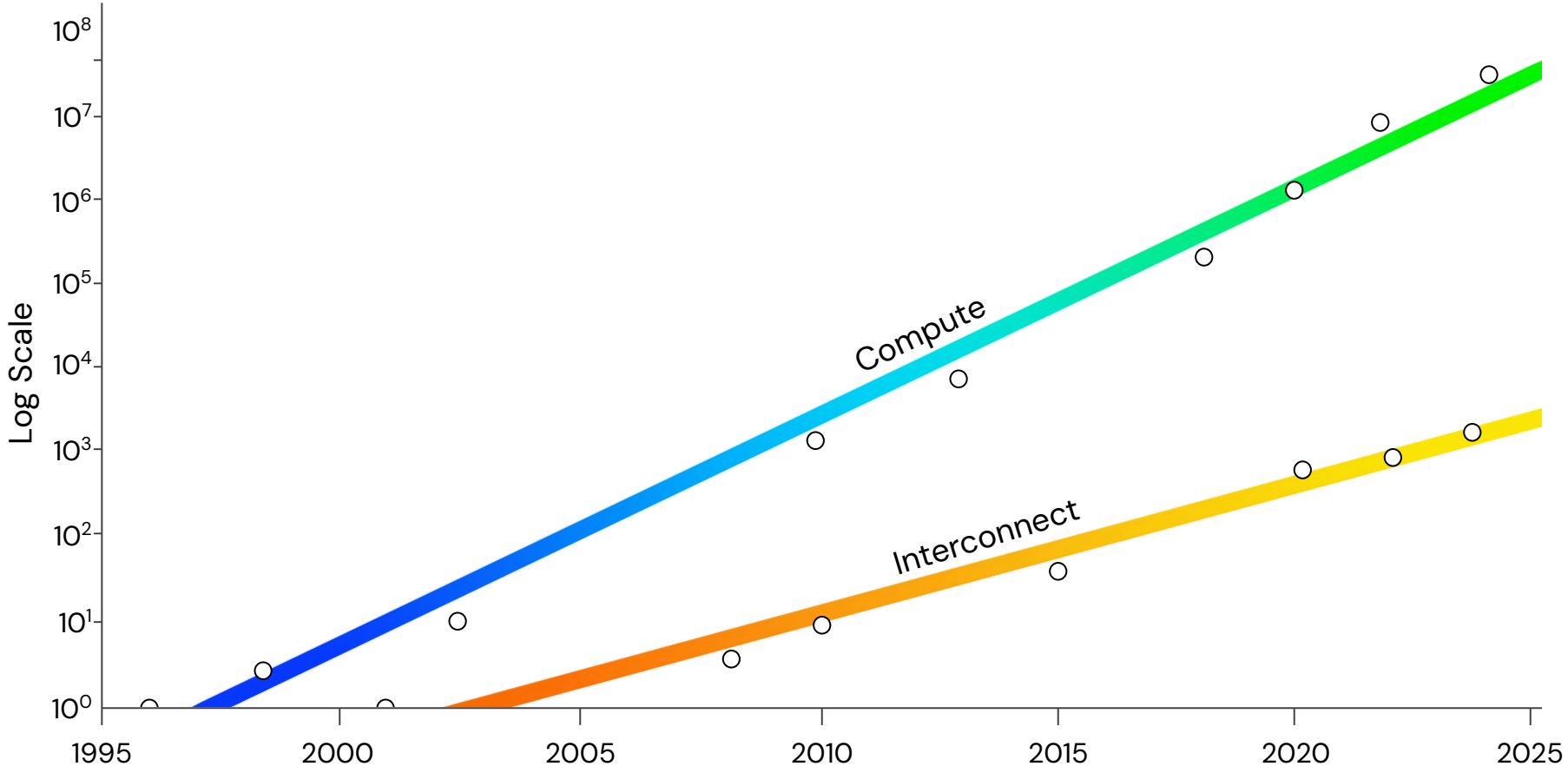
Jessie Rosenberg
Director of Laser Development, Lightmatter

A decade of AI breakthroughs

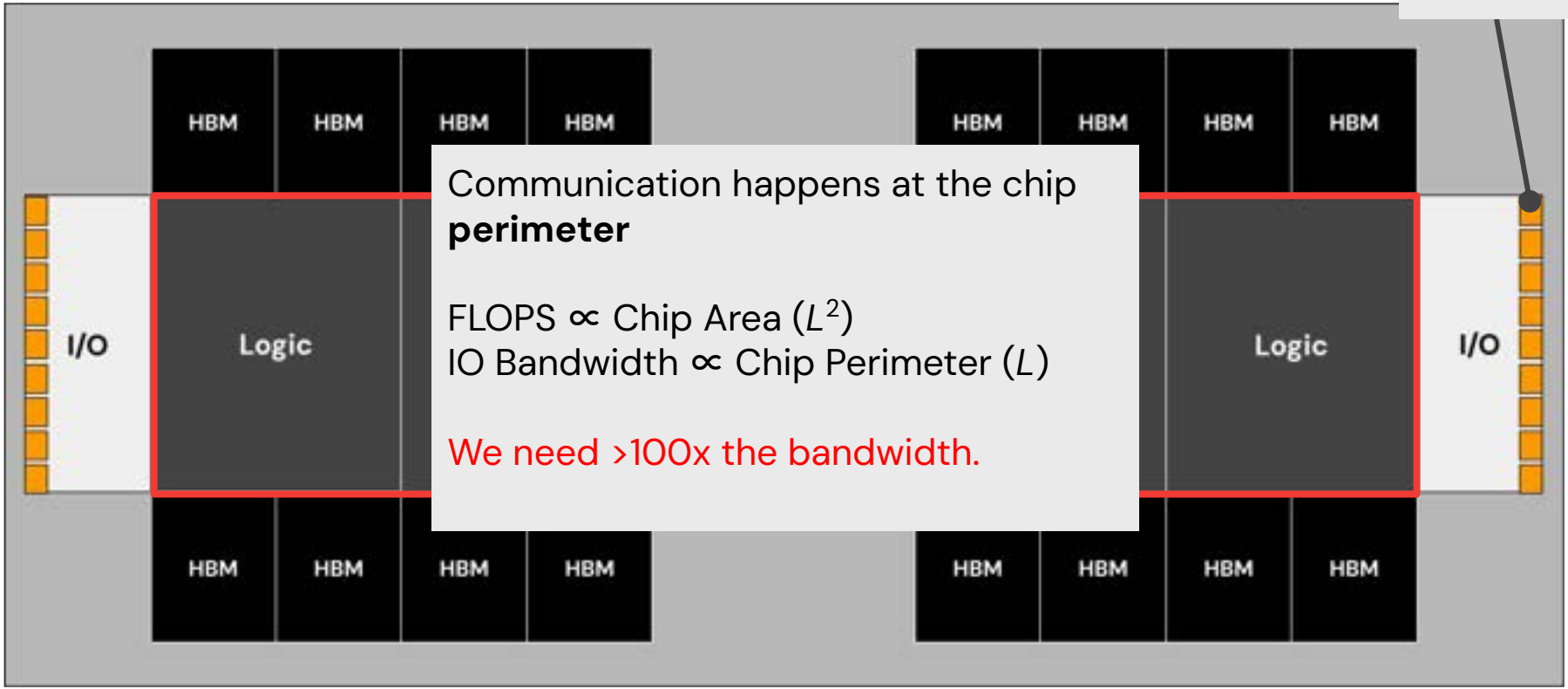
10^9 Growth in a Decade



Interconnect Progress Is Too Slow



Challenge: Package Area and Shoreline



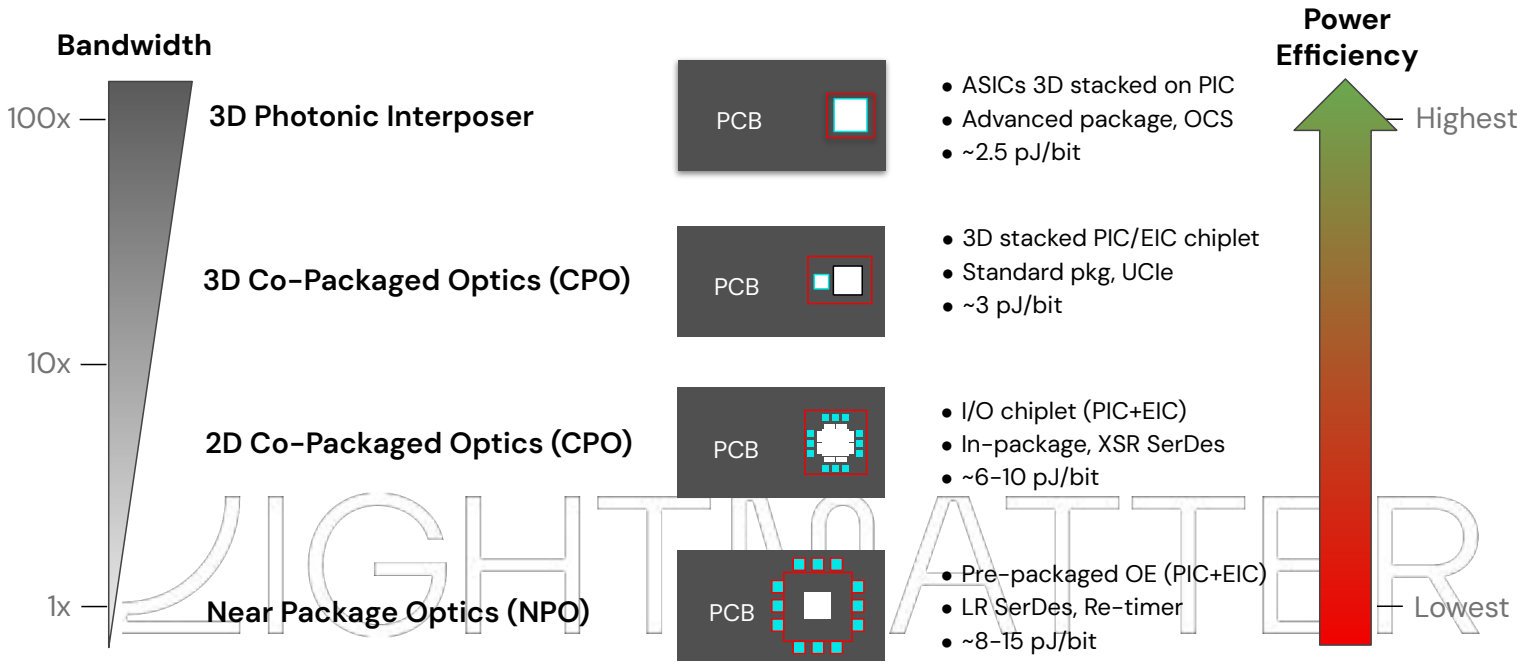
Communication happens at the chip **perimeter**

FLOPS ∝ Chip Area (L^2)
IO Bandwidth ∝ Chip Perimeter (L)

We need >100x the bandwidth.

A new paradigm is needed

Photonics Evolution: Moving Closer to the Chip



Copper, Pluggables

Photonic Integrated Circuit: PIC
Electronic Integrated Circuit: EIC
Optical Engine (OE) = PIC+EIC

About the Speaker

- PhD from Caltech in Applied Physics - Integrated Photonics
  - Some interesting physics around the interactions between optics and mechanics in integrated photonics
- Postdoc & Research Staff at IBM Research - Silicon Photonics
  - Developing silicon photonics from early research to production readiness
- *Interlude*: MIT-IBM Watson AI Lab - AI Algorithms Research & Science Program Manager
  - Fundamental AI research collaboration between industry & academia
- Photonics Architect at Lightmatter - Silicon Photonics
  - Back to silicon photonics roots & combine with AI HW requirements
- Director of Laser Development at Lightmatter
  - Focusing on the critical laser requirements for silicon photonics

Accelerating AI with Light

$850M RAISED

Fidelity	T. Rowe Price
Google Ventures	Matrix Partners
Sequoia	SIP Capital
Spark Capital	MIT
Viking	Stanford

Mountain View (HQ)

Boston

Toronto

300
EMPLOYEES

Nicholas Harris, PhD
Founder, CEO

Darius Bunandar, PhD
Founder, Chief Scientist

Thomas Graham
Founder

Simona Jankowski
CFO

Ritesh Jain
SVP, Engineering & Ops

Bob Turner
SVP, Sales & Solution Arch

Sujatha Wagle
VP, Supply Chain Ops

Beth Keil
SVP, People

Steve Klinger
VP, Product

Boon Tan
VP, Product Engineering

Colin Sturt
General Counsel

Kaushik Patel, PhD
VP, Photonics & Si Eng

Praveen Kukkamalla
VP, Sales

Kurt von Hausen
VP, Cloud Services Sales

Israel Kandarian
Head of Creative Marketing

311
PATENTS

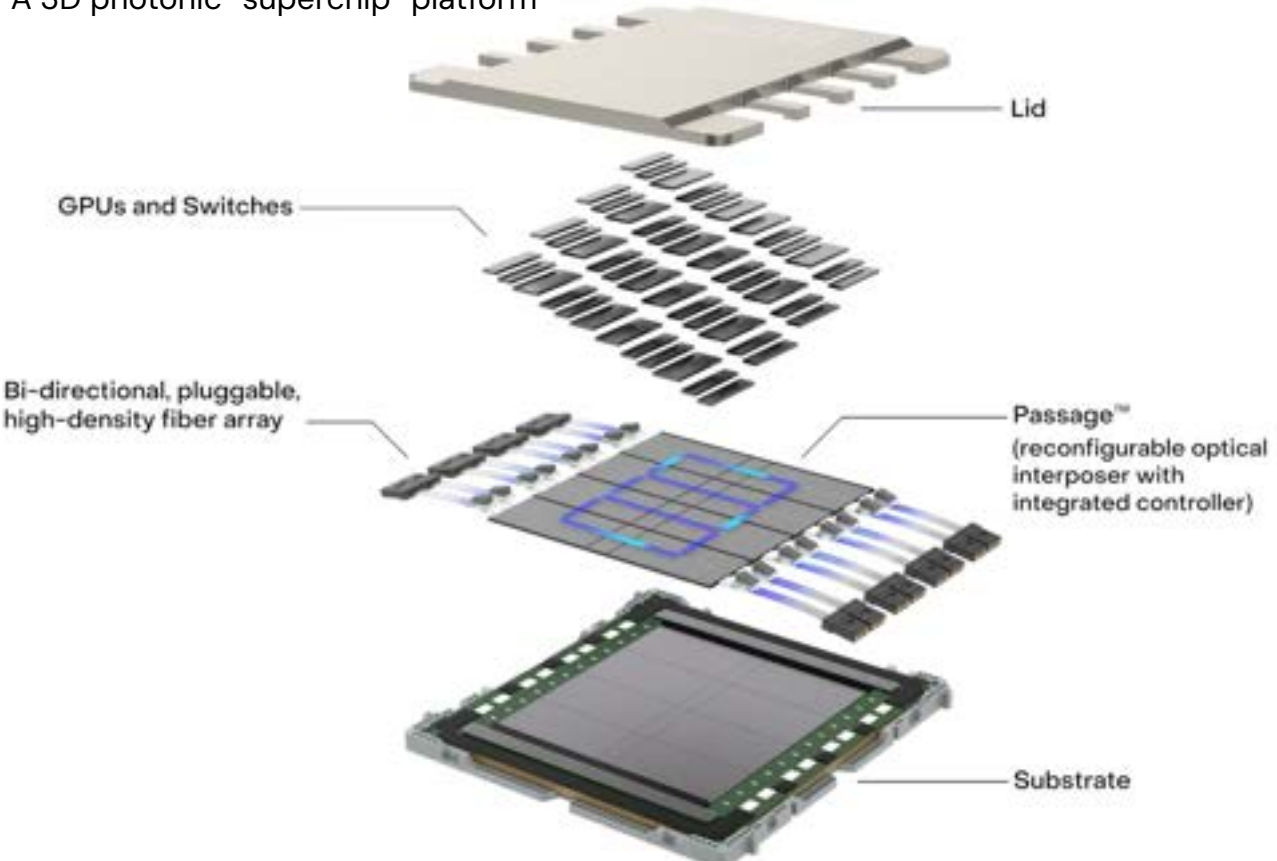
Granted & Pending

Passage™ M Series

A 3D photonic “superchip” platform

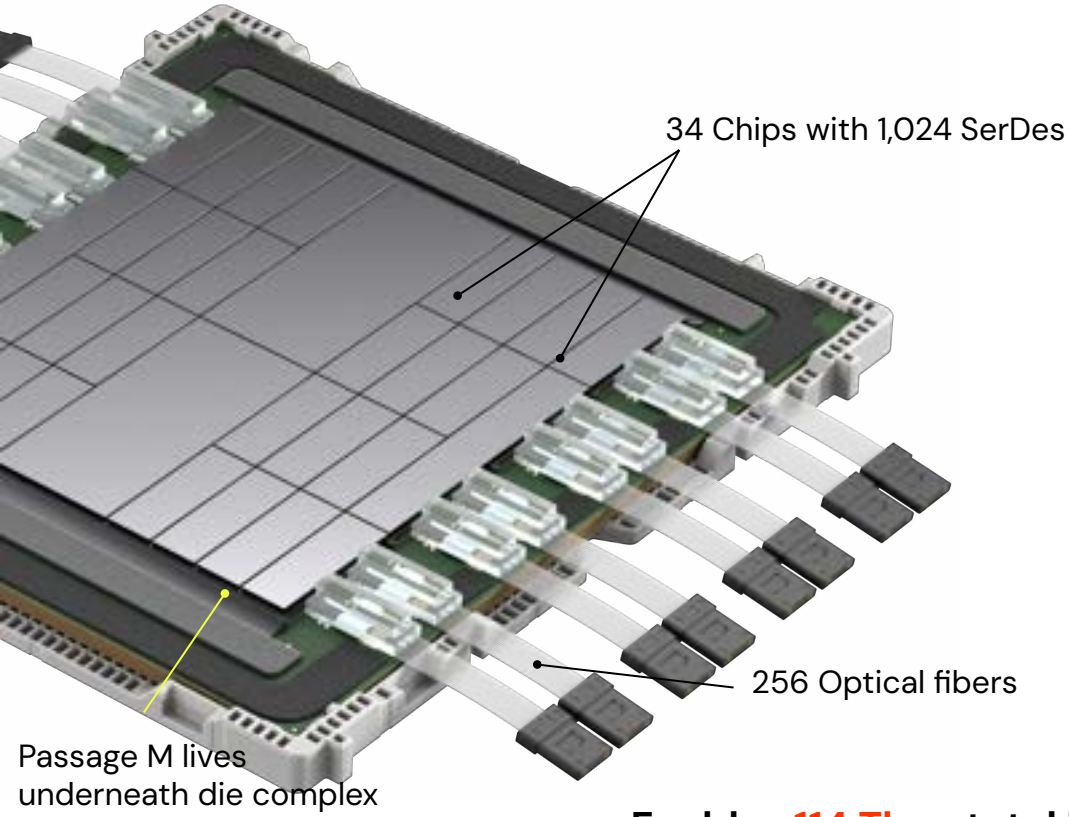
Passage™ M Series

A 3D photonic “superchip” platform



Passage™ M Series

Photonic interposer reference platform

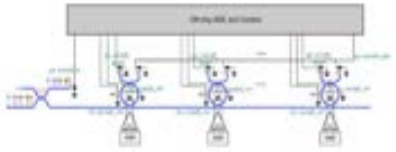


Specifications	
Bandwidth (Tx + Rx)	Up to 114 Tbps
# of SerDes	1024
Silicon die Complex	4,000 mm^2
Power delivery	>1.4 W/mm^2 density
Fibers	256
Redundancy	Optical circuit switching
Substrate Form Factor	91x85mm

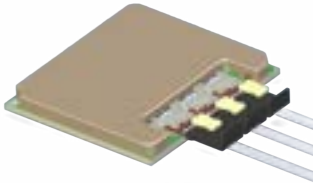
Enables 114 Tbps total bandwidth.

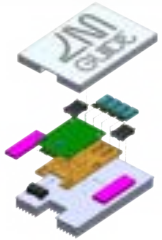
Engineering Capabilities: Rings → Racks

DEVICES



CHIPS



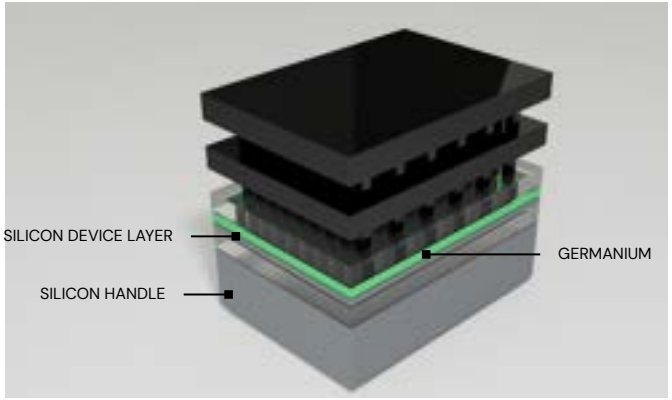


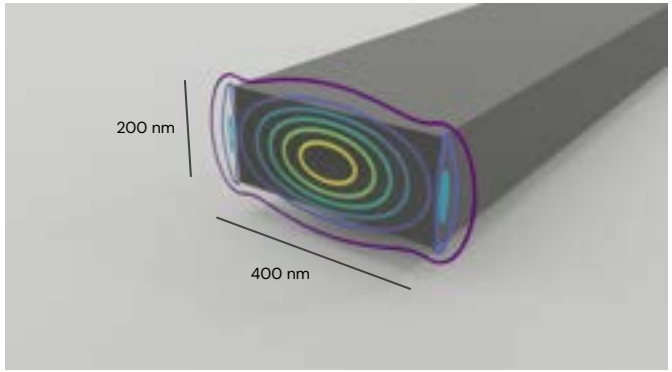
SYSTEMS

DATACENTER

DFX for Photonics Interconnect: **Device**

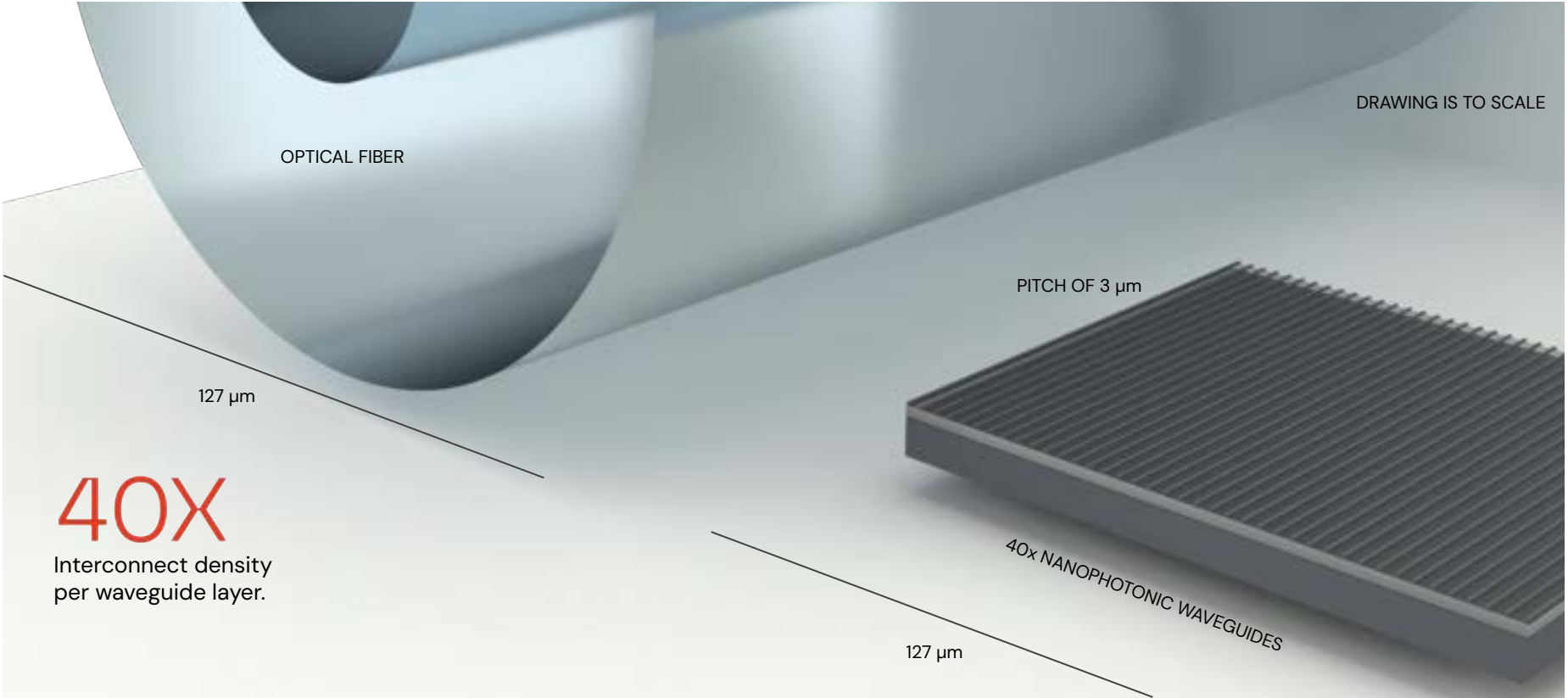
300mm CMOS Fab





A Sense of Scale

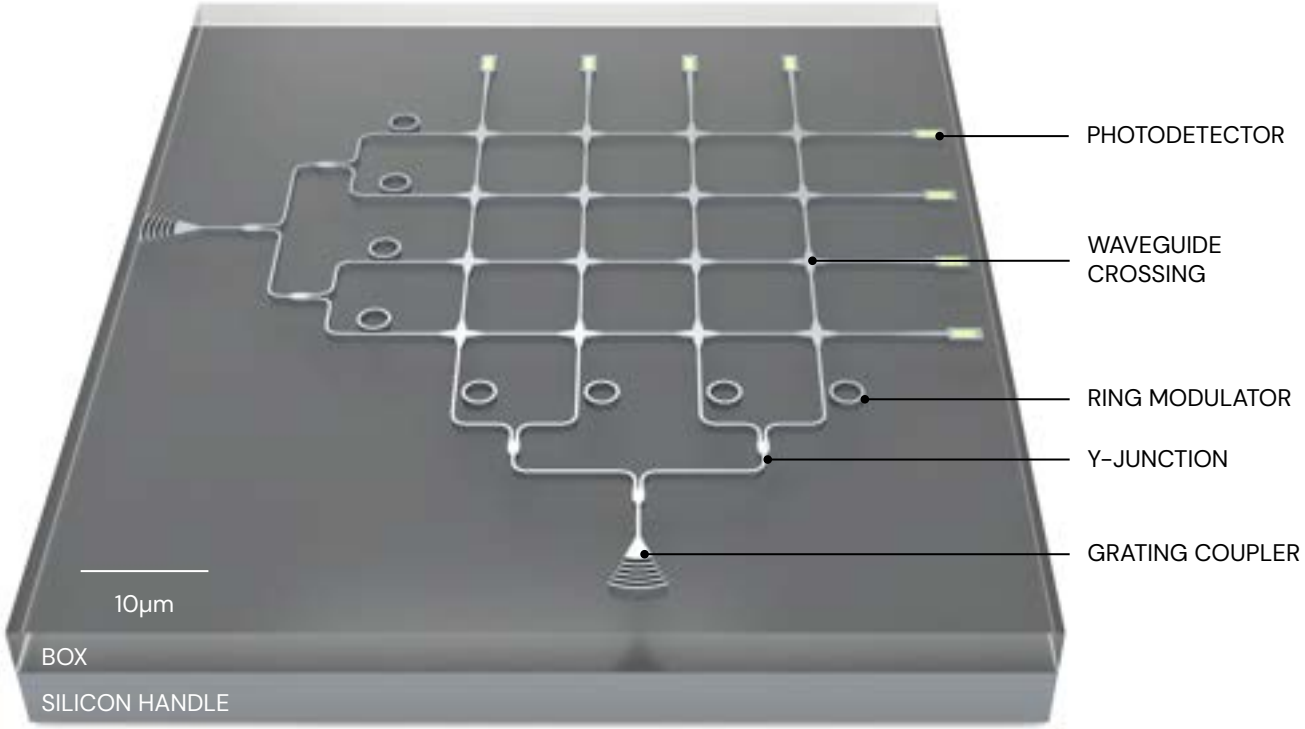
Optical fibers versus nanophotonic waveguides



40X

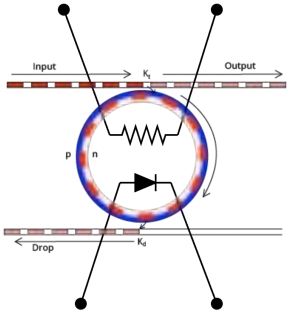
Interconnect density per waveguide layer.

What does silicon photonics look like?

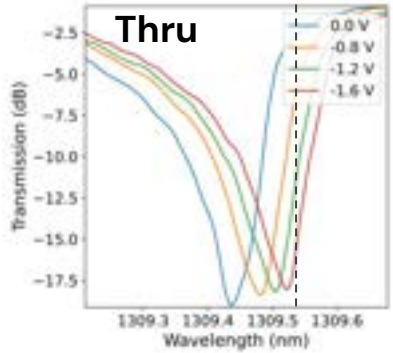


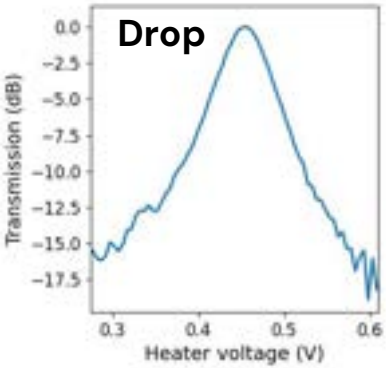
The heart of the engine: silicon microrings

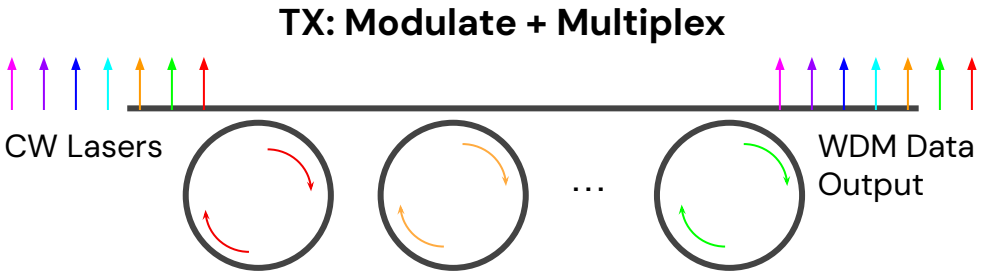
Ultra-compact, high-speed, WDM-friendly

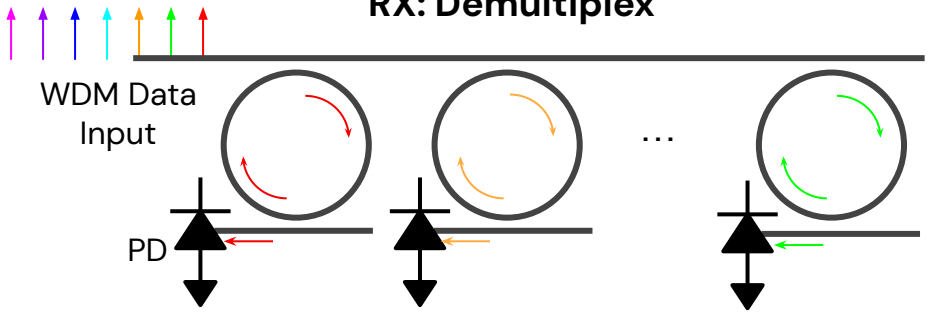


Resistive heater
for tuning
Depletion PN junction
for modulation



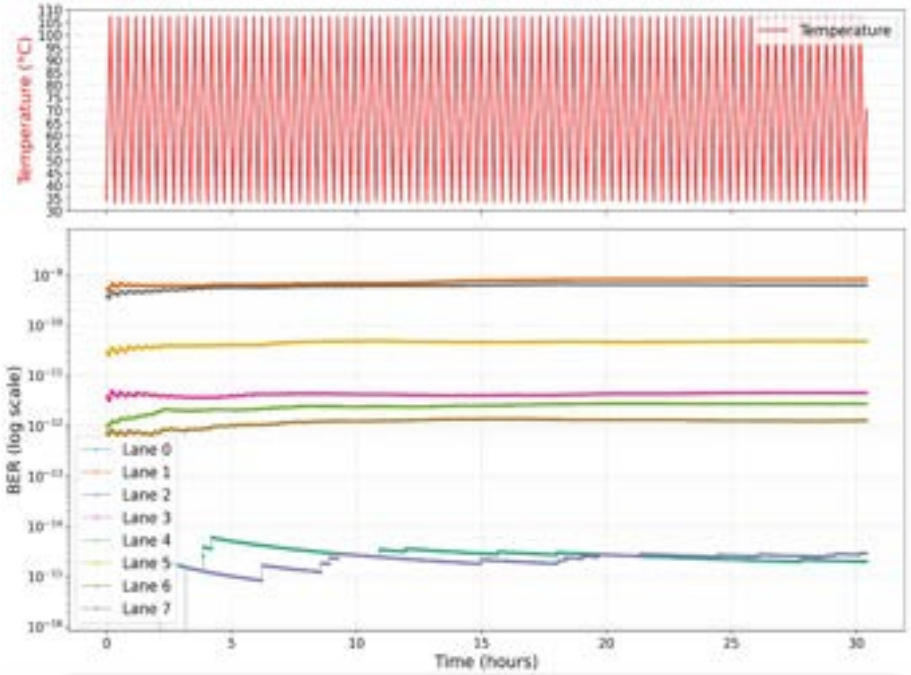


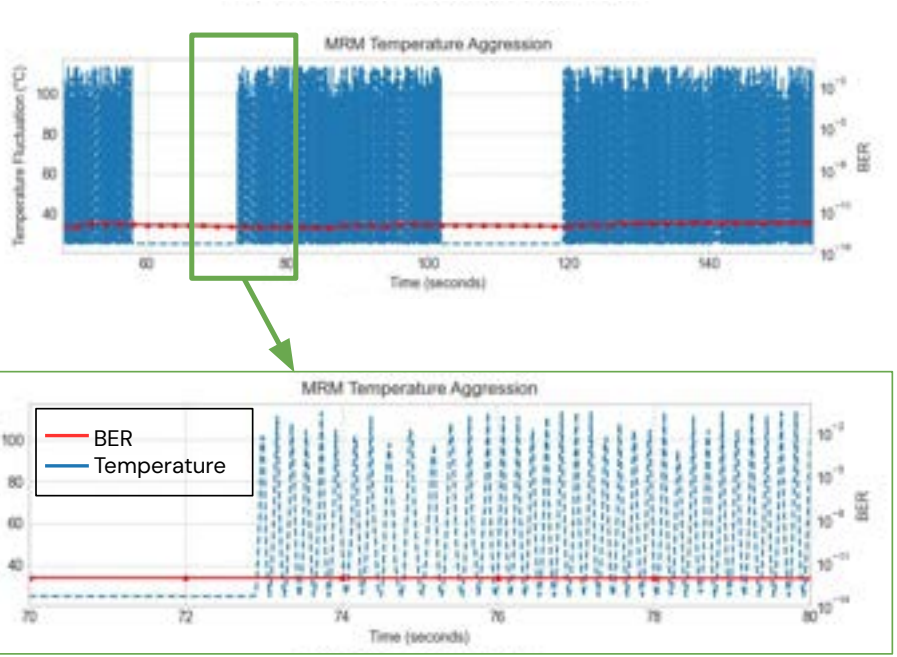




Rock-solid MRMs in extreme thermals

Lightmatter MRM control technology





Measured robustness against 25 →105→25°C (ΔT=80°C) repeated temperature cycling

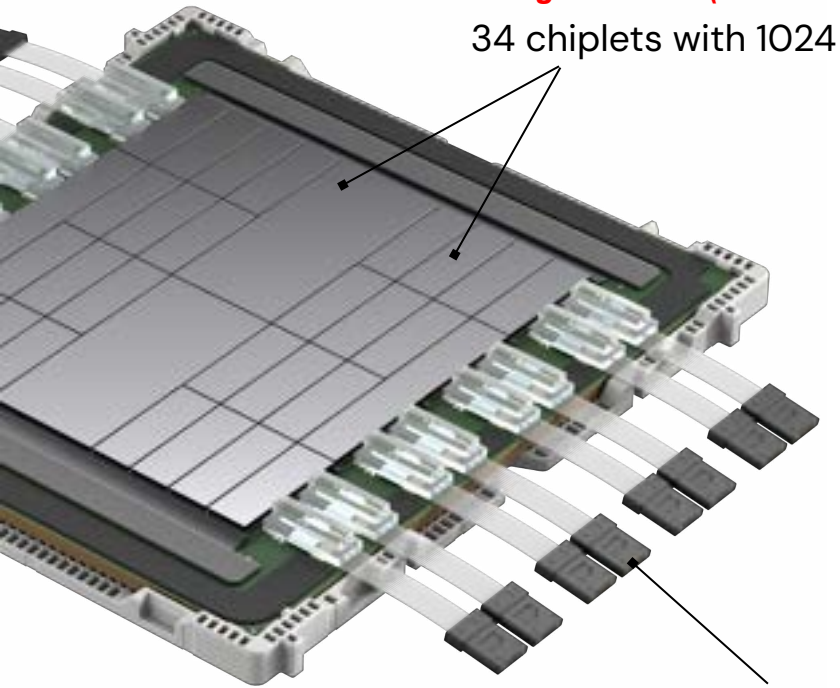
Also robust against rapid 800°C/s temperature change, using an on-die heater aggressor

DFX for Photonics Interconnect: **Package**

Package Level DFX Challenges

Chip & 3D Packaging Yield, Photonics & Electronics Integration, Design for Test (Electrical & Optical)

34 chiplets with 1024 SerDes



256 optical fibers

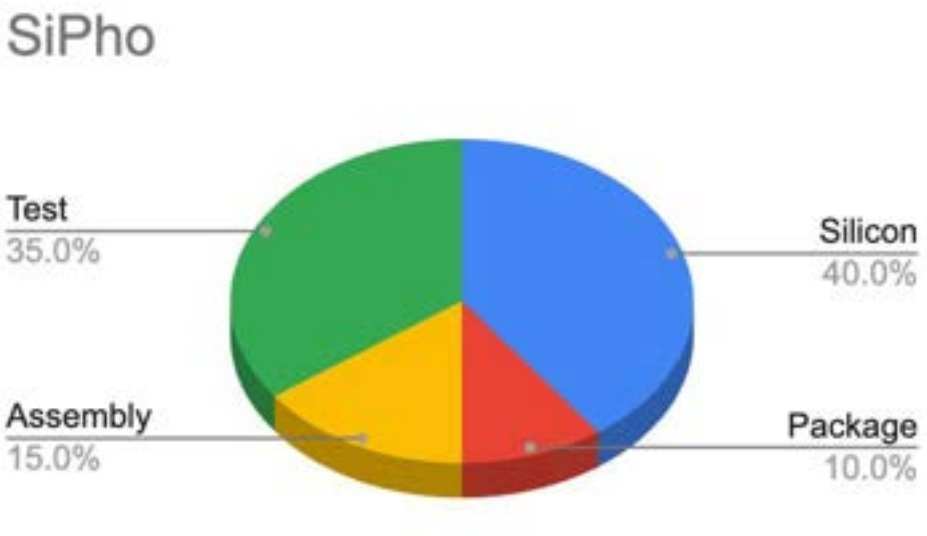
High Precision Alignment, Fiber Attach Yield

Specifications	
Bandwidth (Tx + Rx)	Up to 114 Tbps
# of SerDes	1024
Silicon die Complex	4,000 mm^2
Power delivery	>1.4 W/mm^2 density
Fibers	256
Redundancy	Optical circuit switching

Package Thermals
SI & PI
Reliability

SPAT Costs and the Need for continued Innovation

Silicon, Package, Assembly, Test



Note: Graph shown for demonstration purposes only

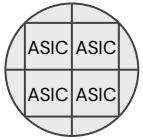
For SiPho Relative Packaging, Assembly and Test (PAT) cost % is increasing

PAT cost challenges in SiPho:

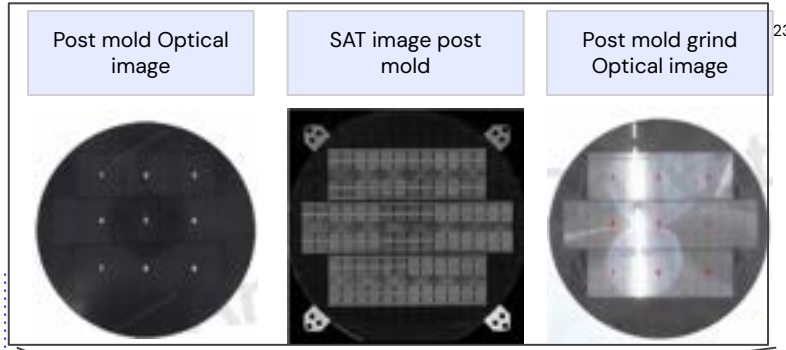
1. In assembly: fiber attach yields
2. In test: test times are much higher

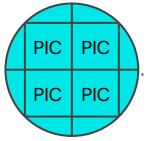
DFM/DFT-driven product architecture is must for high volume SiPho manufacturing and cost reduction

M1000 How it's built.



ASIC





Wafer Test

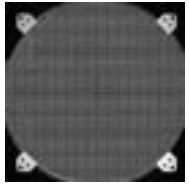
TSV Reveal

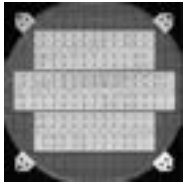
RDL and bumping

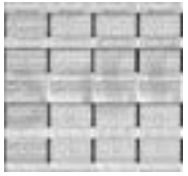
CoW reflow: PIC wafer (TSV) to ASIC attach

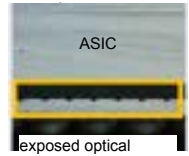
Wafer level underfill, mold and grind

Wafer dicing









exposed optical waveguide in the PIC

System

Final Electro- optical test

Fiber attach with real time optical test

Package e-test (Known good PKG)

Heat sink attach

Post substrate attach reflow

LM Packaging, Test, Quality and Reliability Methodology

Concept/Development

- SI/PI
- Substrate Design
- Design for manufacturing/Reliability
- Thermal analysis
- Mechanical Design/Analysis
- Optical Analysis

Assembly/Test

- 2D and 3D Heterogeneous Integration & process dev.
- Wafer Electrical Sort and Optical Characterization
- Wafer and component test points through the process flow

Reliability/Validation

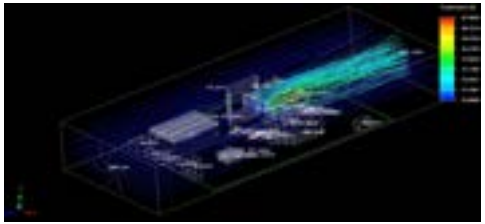
- Electrical and Compliance Tests – ESD, Latch Up, EMI/EMC
- Package/Environmental – TC, UHAST, HTS, S/V, Fiber Integrity
- Operational – HTOL
- Failure rate and Lifetime prediction

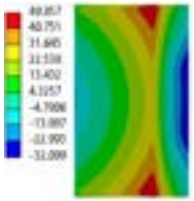
Analysis and Lab Validations

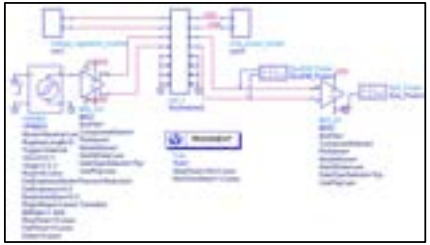
Deliver an **error free** and **high quality design**
Model **validation** with lab experiments
Scale **reliable** solutions to High Volume Manufacturing

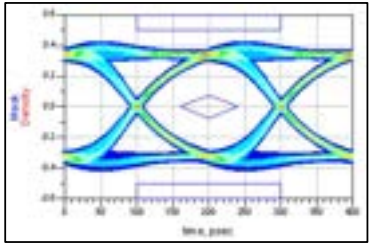
Capture Multi-Physics Interactions

Optical Design	• Waveguide mode analysis • Coupling efficiency • Link budget analysis.
Signal Integrity	• Insertion loss • Return loss • Crosstalk analysis
Mechanical Design	• Stress and strain analysis • Warpage and shock/vibration analysis.
Thermal Design	• Airflow simulation • Thermal analysis from silicon to rack level
VR / Power Integrity	• IR drop analysis • AC/Impedance analysis • Transient analysis









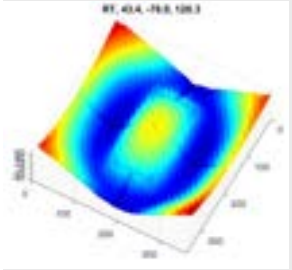
Thermal, Mechanical, and Optical Analysis

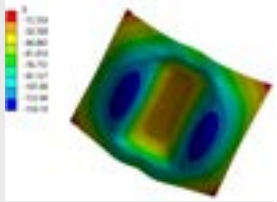
Mechanical Analysis

Warpage analysis for to optimize fiber attach manufacturing

Model

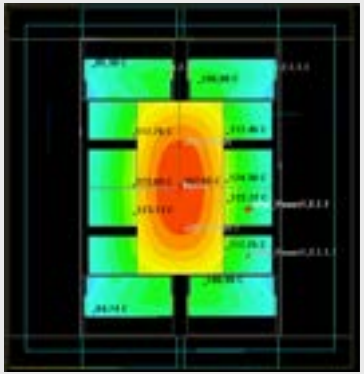
Measurement





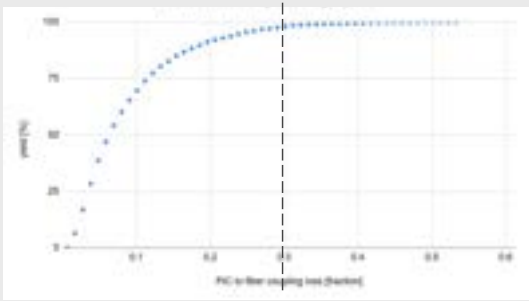
Thermal Analysis

Heat transfer based design rule definition for 3D Heterogeneous Integration

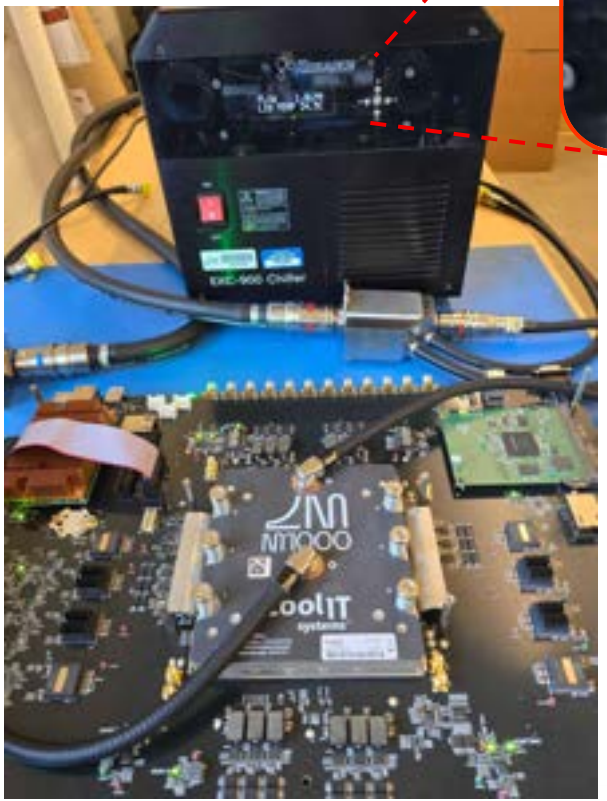


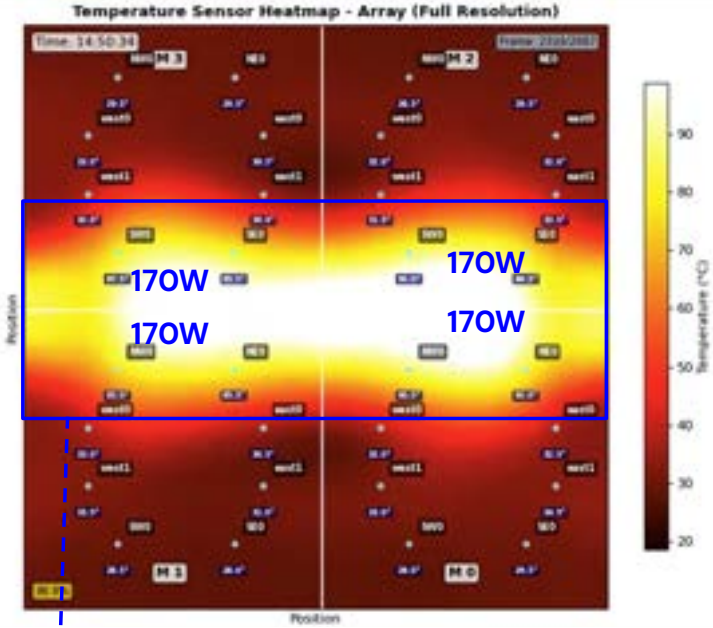
Optical Analysis

Zemax + Lumerical analysis to define manufacturing tolerance to meet yield



Power delivery and thermal load

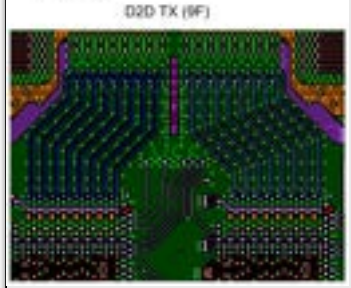




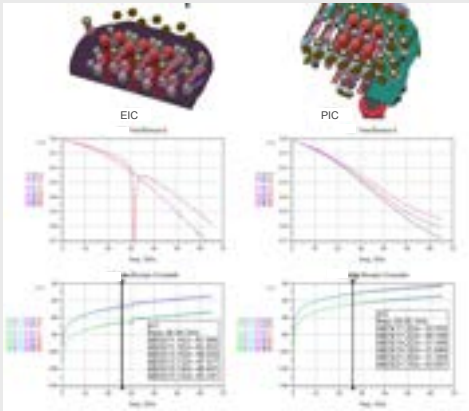
369mm^2 thermal test chip, power density 1.47W/mm^2.
Passage TSVs support >2.5A/mm^2.

SI, PI + Packaging Design

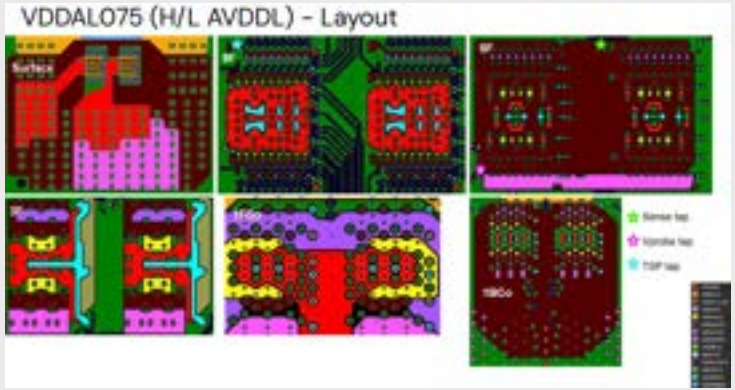
Line Side Routing

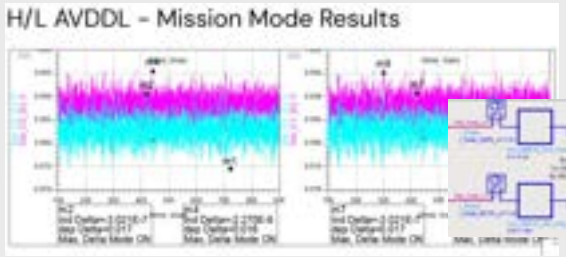


Bump & uVia XTALK optimization



Power Integrity

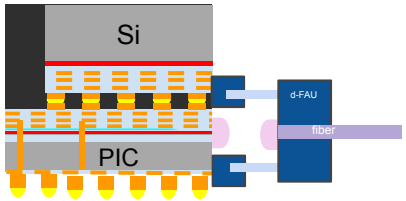




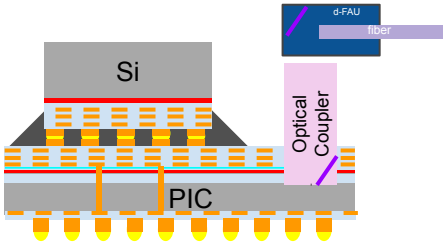
Fiber Attach Methods

Traditional FAU

Lens based edge attach



Wafer Level Optical coupler



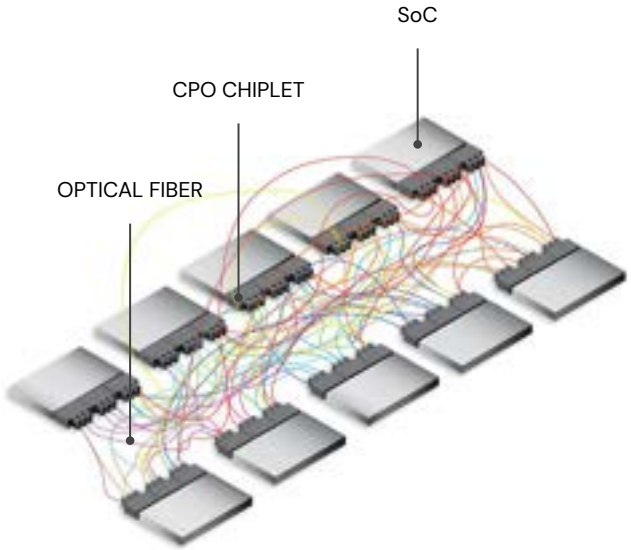
V-Groove based Fiber Attach Methods	**Lens based: Detachable fiber attach**	**LM Focus: Detachable fiber attach**
Package level assembly (interface on die edge)	Package level assembly (interface on die edge)	Wafer level assembly and test compatible
Not compatible with 3D Arch	**Compatible with 3D Package Arch**	**Compatible with 3D Package Arch**
XPU to OE D2D: Standard Package	**XPU to OE D2D: Standard & Adv. Package**	**XPU to OE D2D: Standard & Adv. Package**
Passive or Active alignment	Active alignment	Passive or Active alignment
Test with FAU after package assembly	Test with FAU after package assembly	Test with FAU at wafer level
FAB: GF only	FAB: GF & TSMC	FAB: GF & TSMC
Serviceability: No	**Serviceability: Yes**	**Serviceability: Yes**
Limited scalability to HVM	Scalability to HVM	HVM scalable solution

LM driving strong ecosystem partnership to bring detachable FAUs to HVM scale

DFX for Photonics Interconnect: **System**

System Level DFX Challenges

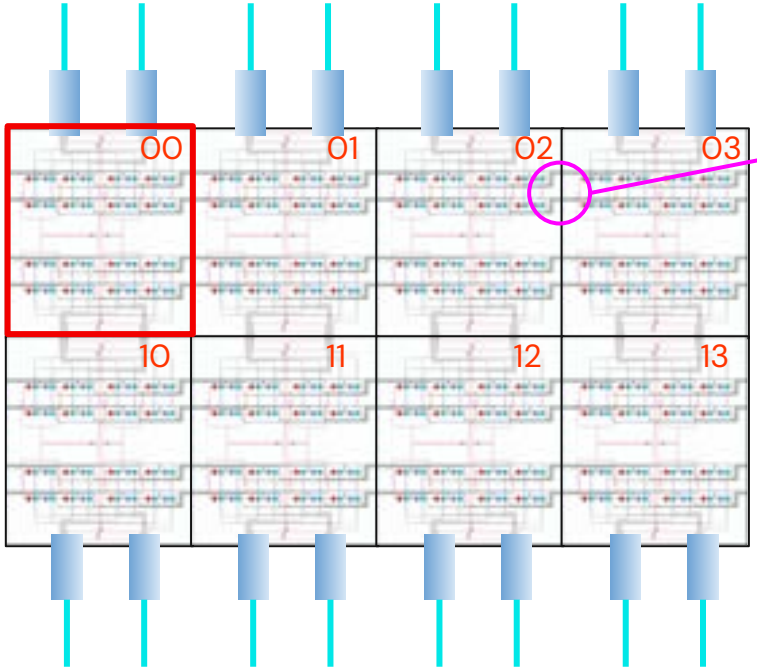
SERVICEABILITY, MANUFACTURABILITY, YIELD



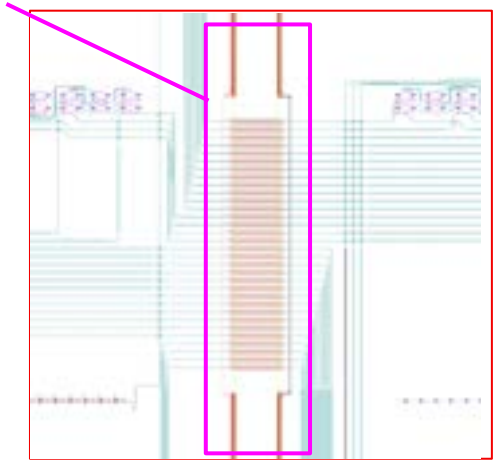
CO-PACKAGED OPTICS ALL-ALL

Reconfigurable connectivity

A dynamic, programmable optical fabric in the 2x4 tile design



Photonic cross-reticle stitching

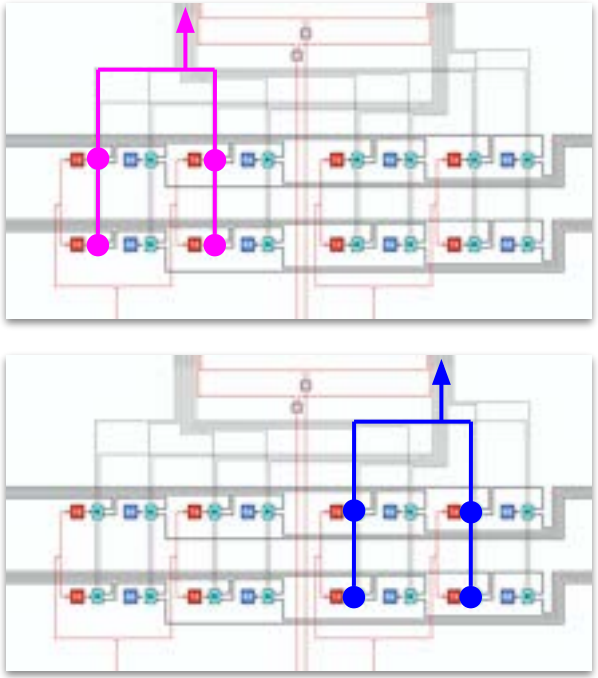


Passage M1000
2x4 tile

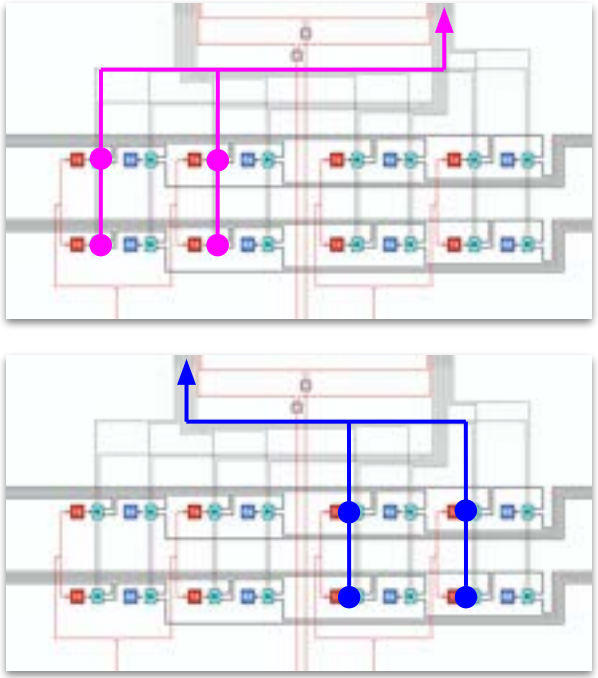
Resilience through optical circuit switching

Fiber attach redundancy allows users to route around failures

Option A (default):



Option B (backup):

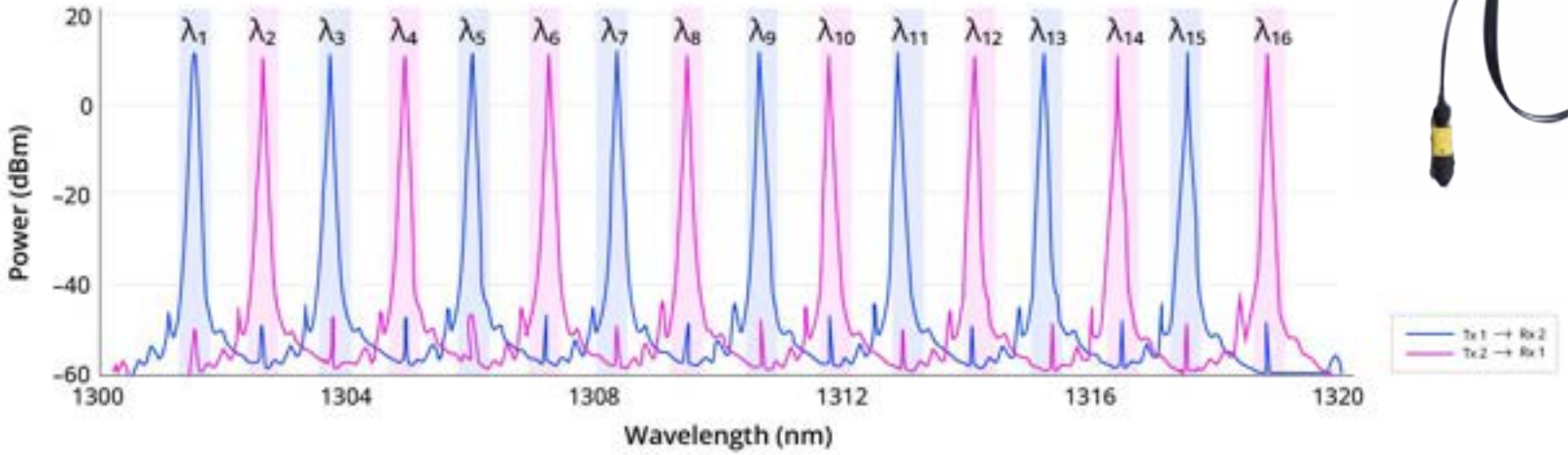


Guide™: External WDM laser

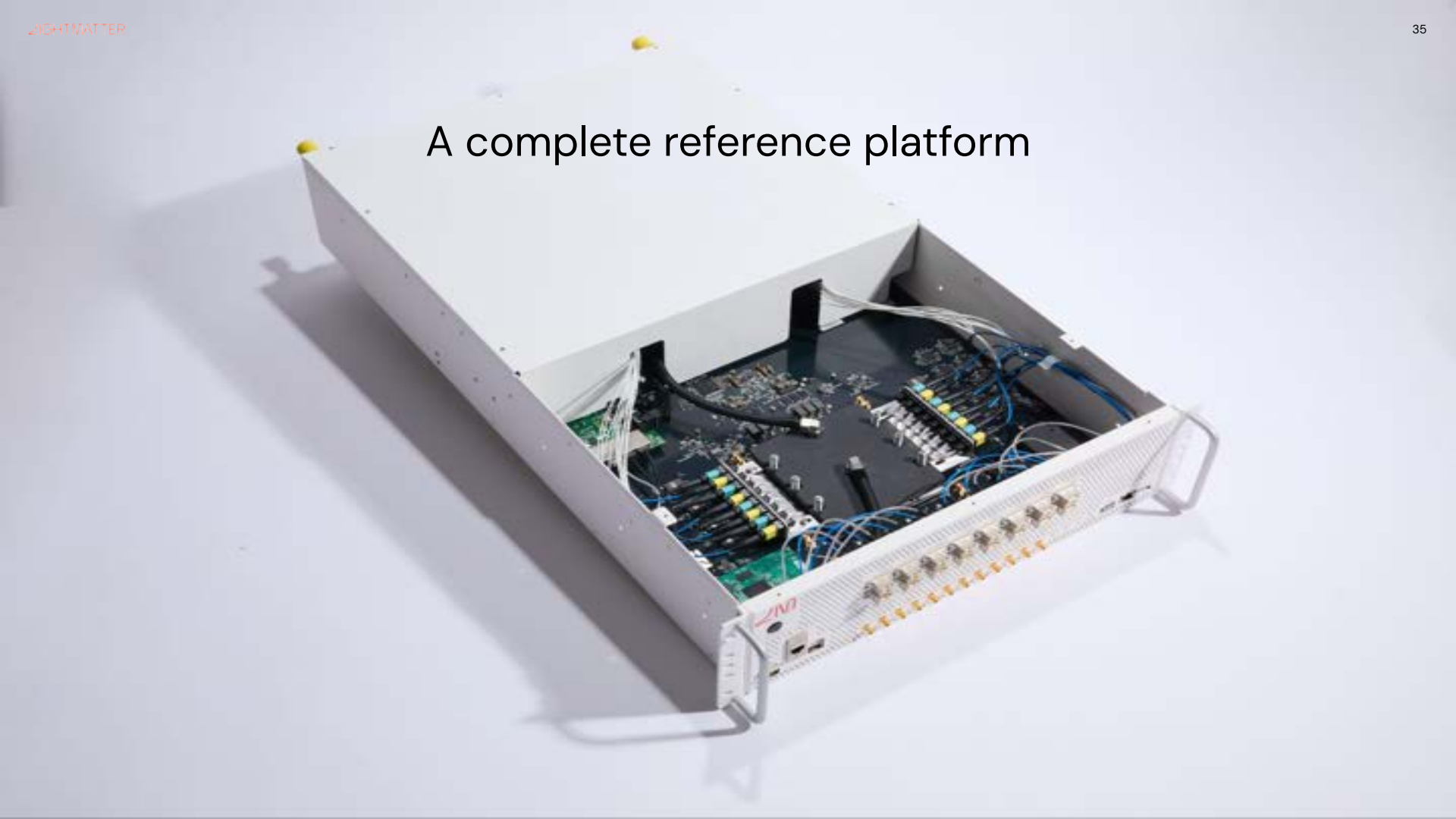
Up to 16 wavelengths per fiber, 200 GHz grid

16 fiber output

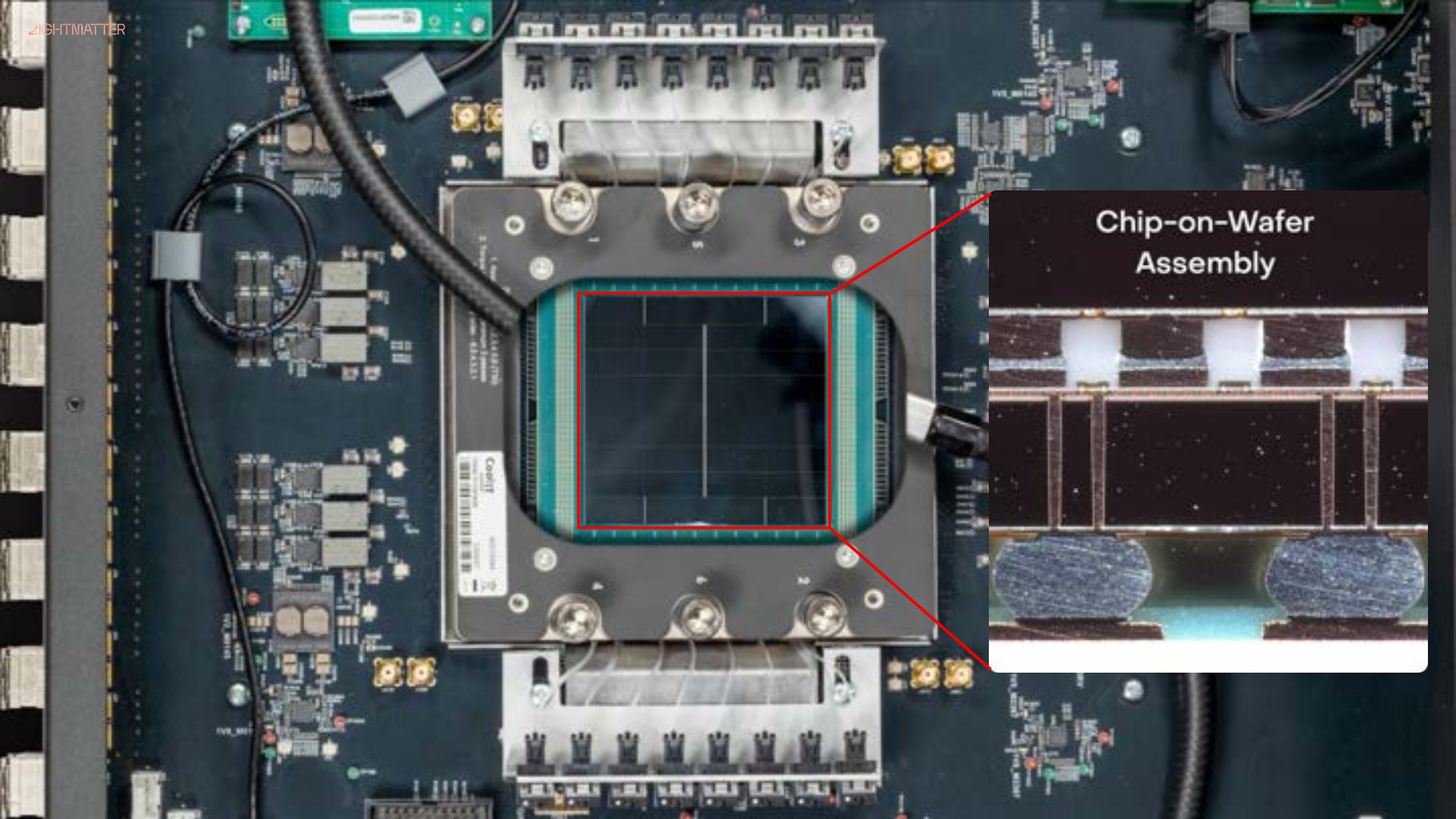
Optimized for microring modulator Tx architectures



A complete reference platform




M1000
CoolIT
systems


Chip-on-Wafer
Assembly

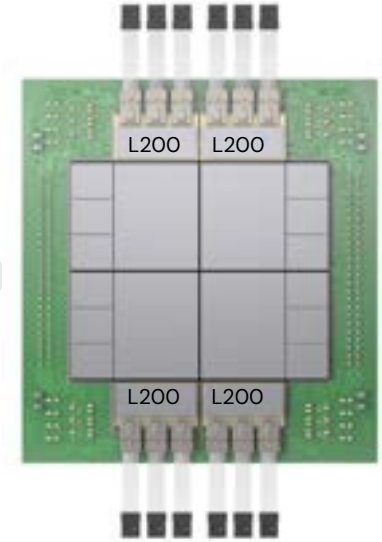
Lightmatter 3D CPO Product and Ecosystem

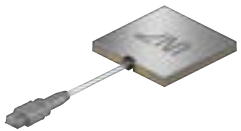
Customer ASIC with UCIe IP	**Multiple fabs**
Passage™ EIC Partners	tsmc
LIGHTMATTER Passage™ PIC	tsmc
Detachable Fiber Coupler	**Multiple Suppliers**

Guide™ Light Engine (16λ, 100 mW/fiber)

ASE

Amkor Technology





- Global ecosystem
- High-volume readiness
- Quality and reliability

Key Takeaways

- Transition from traditional manufacturing to **specialized skills**
- Working **cross-functionally** is key - make connections!
- Opportunities to go **broad** or **deep**
- New industries provide **new opportunities**

THANK YOU