LIGHTMATTER

Photonic-Enabled Heterogeneous Integration: The Future of AI System Scaling

Sandeep Sane, Ph.D.
Senior Director, Head of Packaging Technologies

SEMICON® TAIWAN

$850M RAISED

Fidelity
Google Ventures
Sequoia
Spark Capital
Viking
T. Rowe Price
Matrix Partners
SIP Capital
MIT
Stanford

3
OFFICES

Mountain View (HQ)

Boston

Toronto

300
EMPLOYEES

Nicholas Harris, PhD
Founder, CEO

Darius Bunandar, PhD
Founder, Chief Scientist

Thomas Graham
Founder

Simona Jankowski
CFO

Ritesh Jain
SVP, Engineering & Ops

Bob Turner
SVP, Sales & Solution Arch

Sujatha Wagle
VP, Supply Chain Ops

Beth Keil
SVP, People

Steve Klinger
VP, Product

Boon Tan
VP, Product Engineering

Colin Sturt
General Counsel

Kaushik Patel, PhD
VP, Photonics & Si Eng

Praveen Kukkamalla
VP, Sales

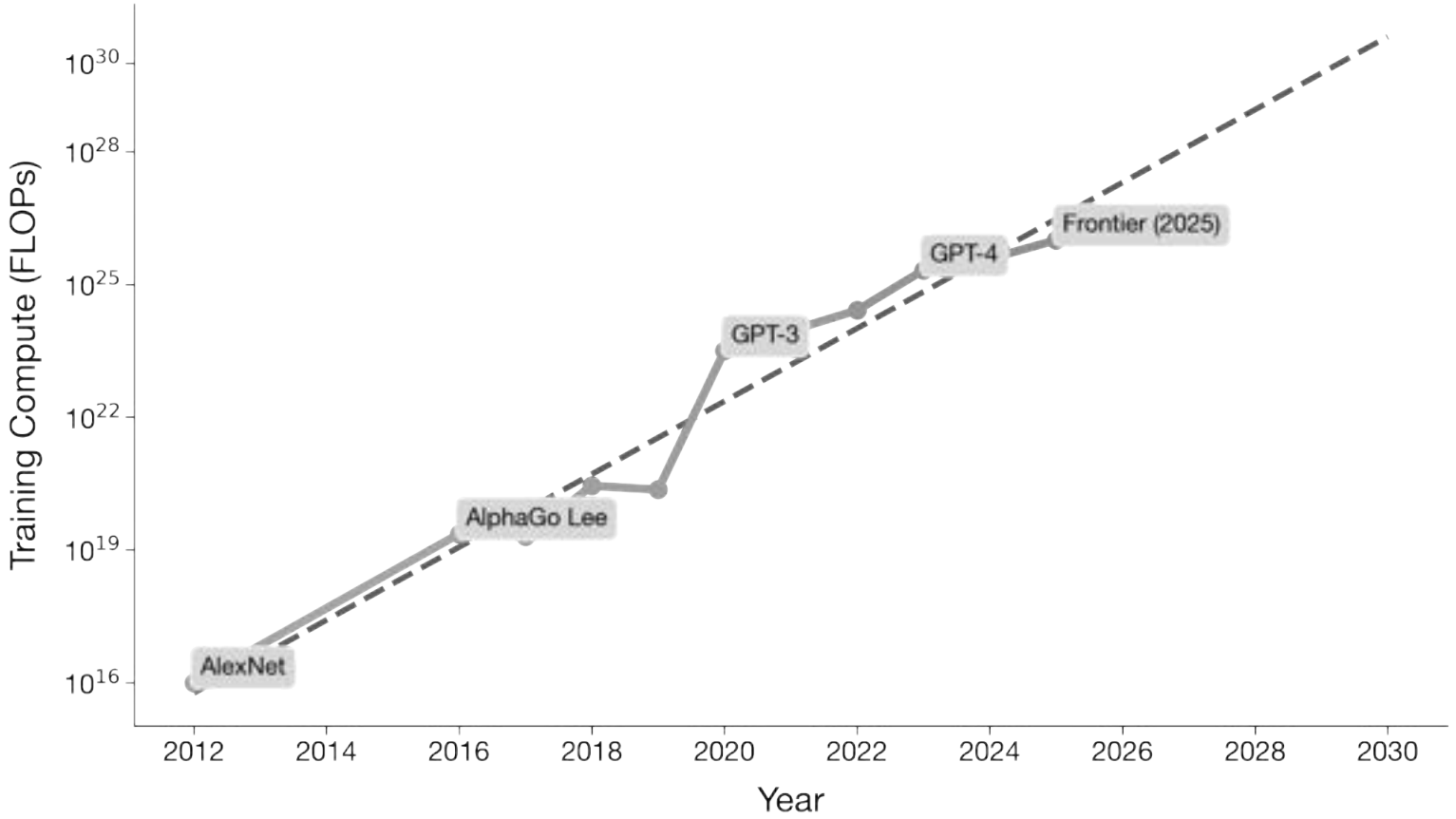
Kurt von Hausen
VP, Cloud Services Sales

Israel Kandarian
Head of Creative Marketing

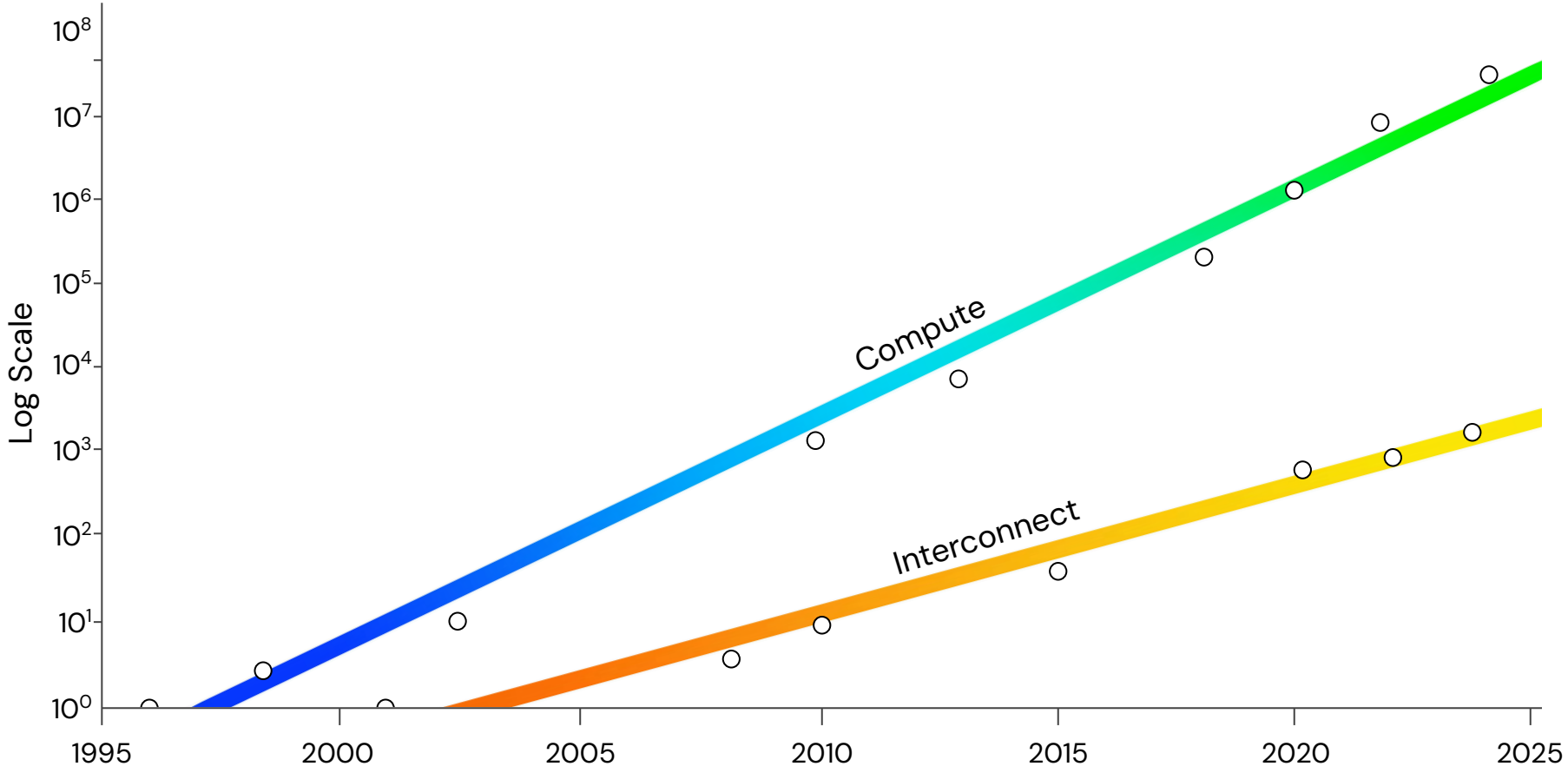
311
PATENTS

Granted & Pending

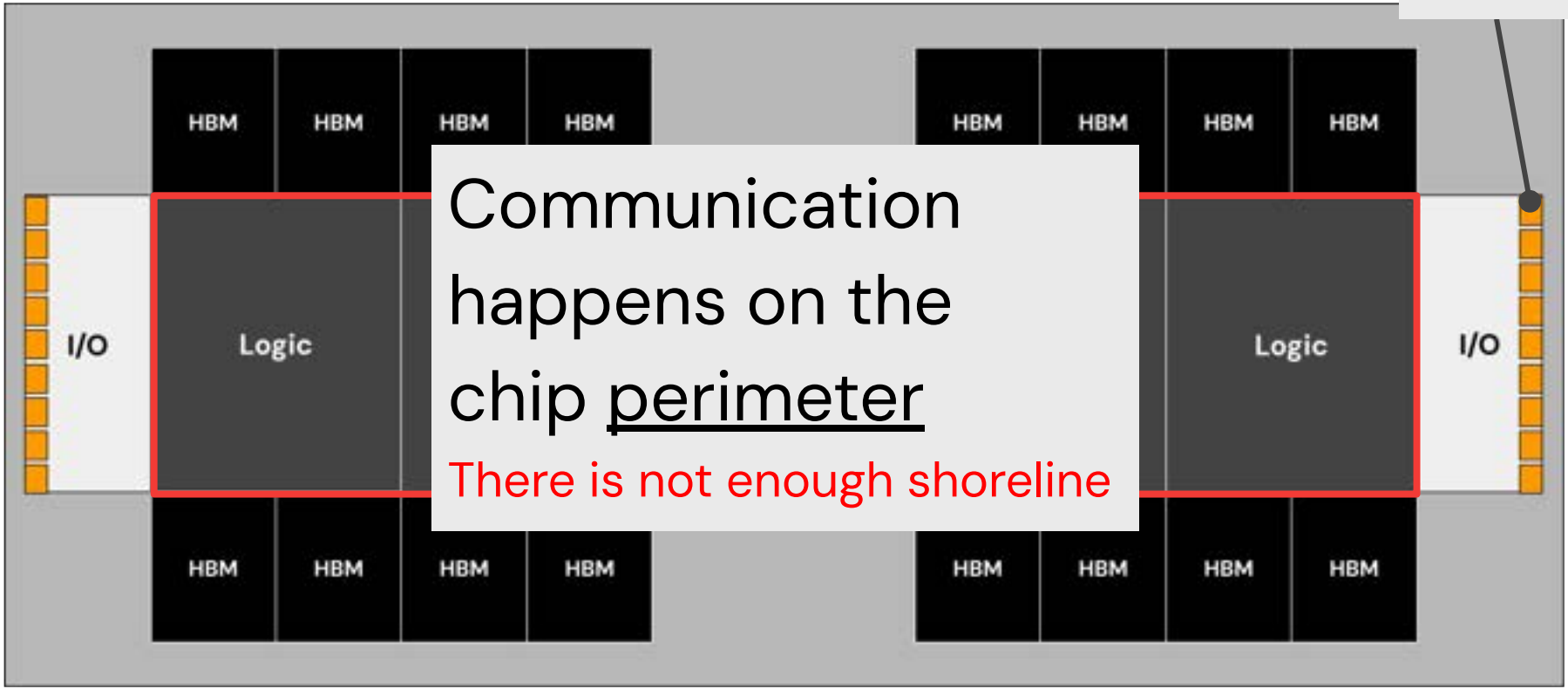
10^9 Growth in a Decade



Interconnect Progress Is Too Slow

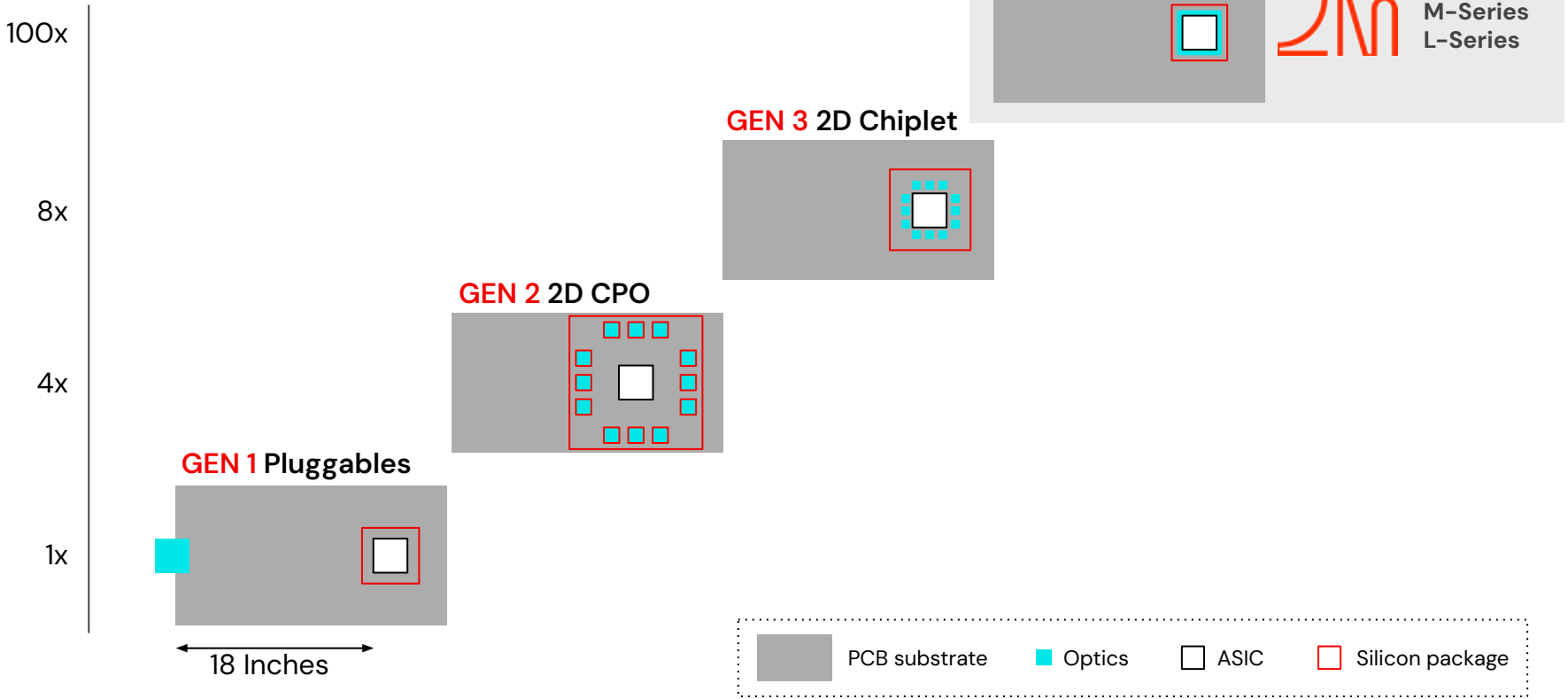


Challenge: Package Area and Shoreline

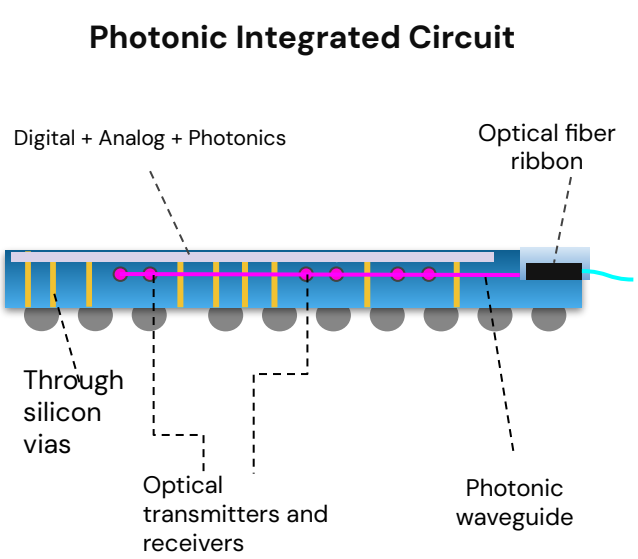


A new paradigm is needed

Photonics Evolution: Moving Closer to the Chip

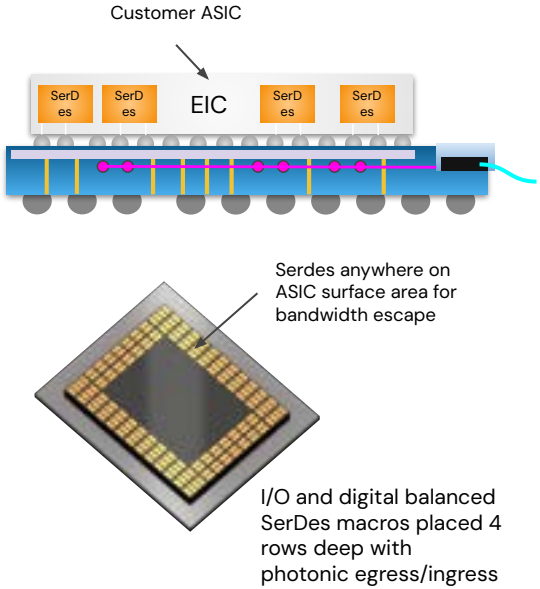


Passage ™ : 3D Photonic Interposer

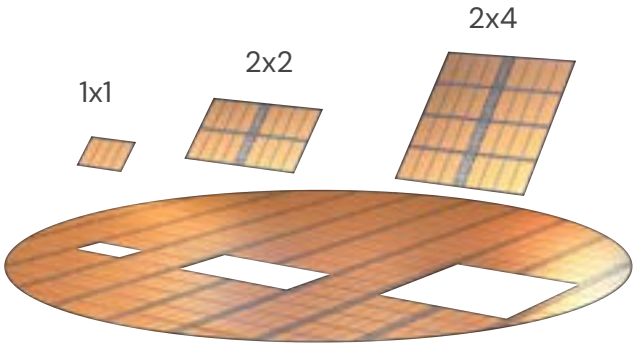


Passage Cross Section

(note: digital/analog can be integrated in top die; FAB choice dependent)



Passage value (3D integration) and density

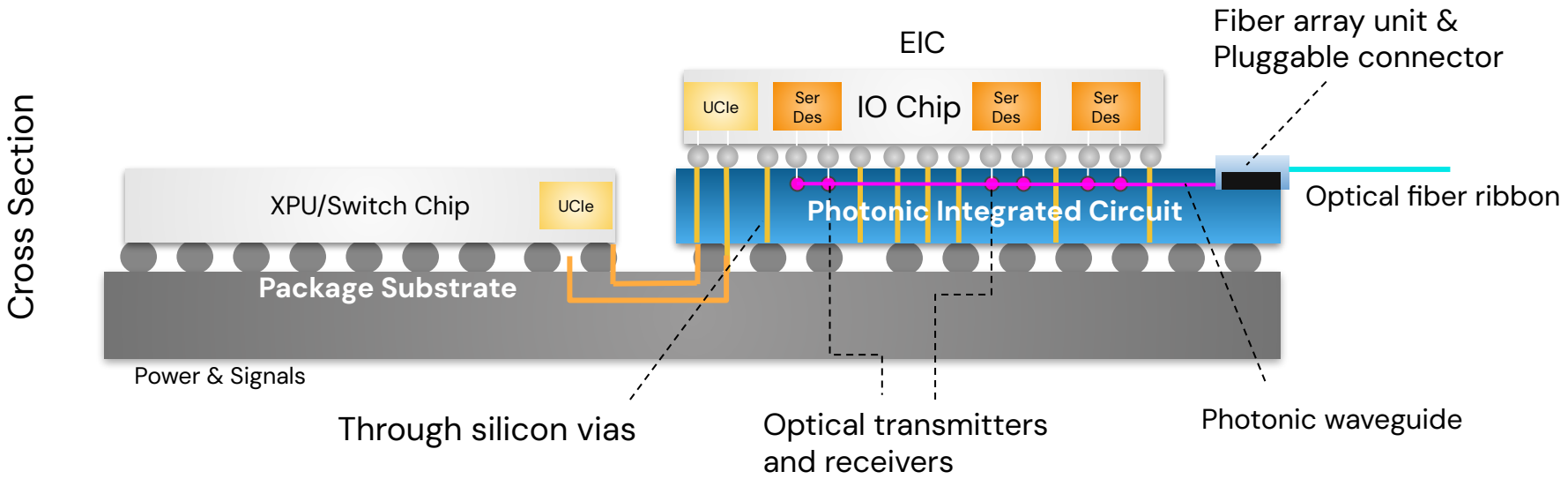


Passage scalability from single to multi-reticle

Built on 3D packaging technology and a Chip-on-Wafer assembly flow

3D CPO Requires Compact Optical Modulators and Receivers

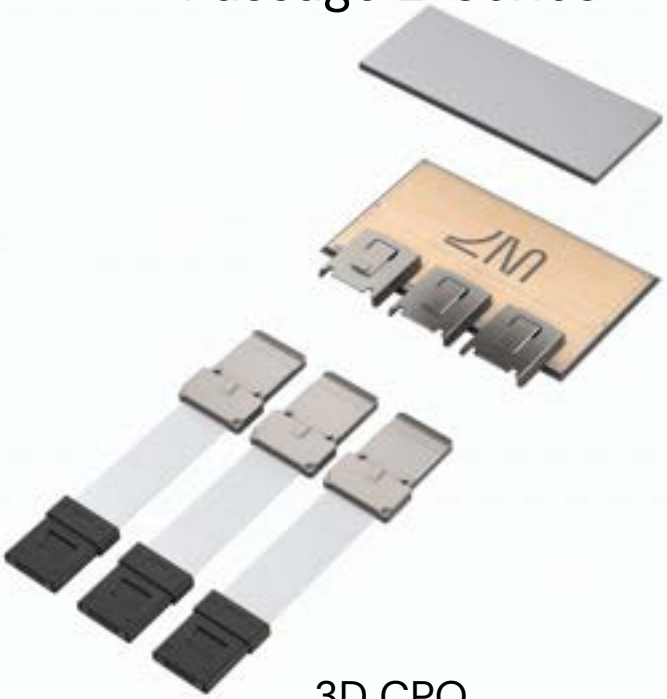
Standard Package Example



Standard processes today

- Bump pitch: ~120 μm
- Bump size: ~80 μm
- **Area for a transmitter/receiver: 0.015 mm²**

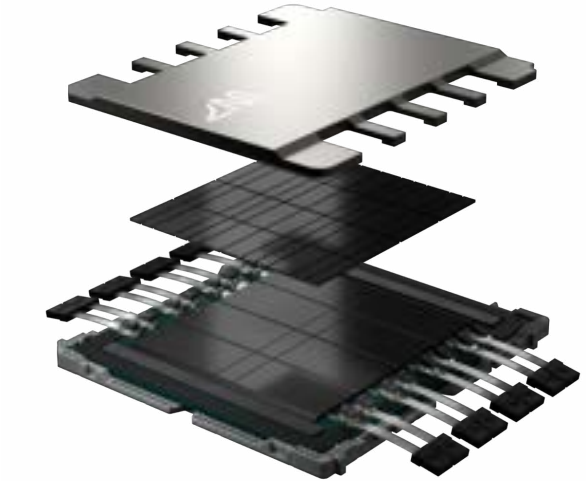
Passage L-Series



3D CPO

Available 2026

Passage M-Series

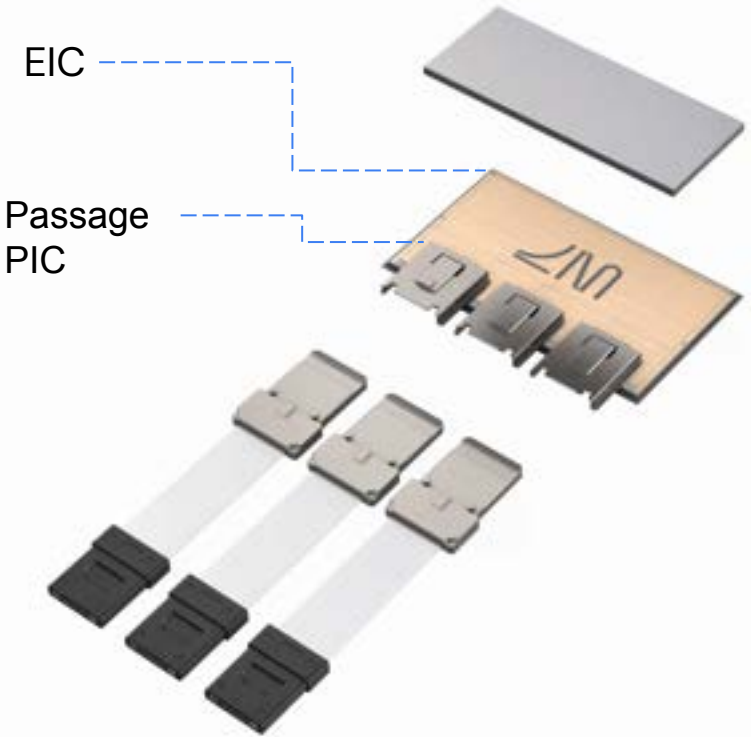


Photonic Interposer

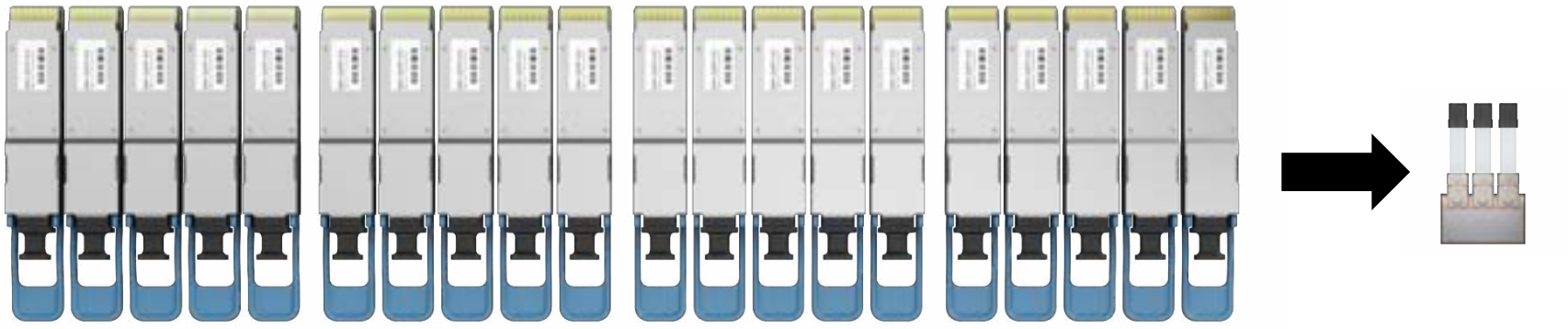
Available Now

Passage™ L-series 3D CPO

- Single reticle
- I/O EIC with UCIe & SerDes
- >1.5 Tbps/mm bandwidth density
- Detachable FAU



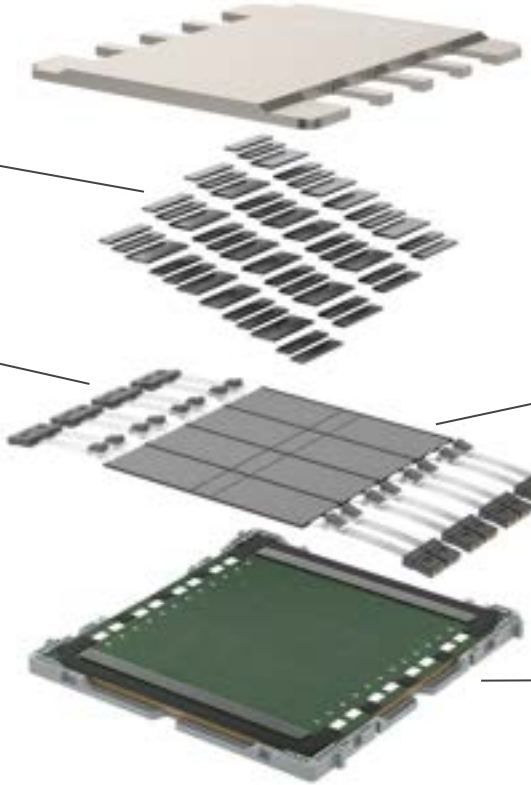
20 pluggables in the area of a quarter.



1.6 Tbps pluggables

L-Series

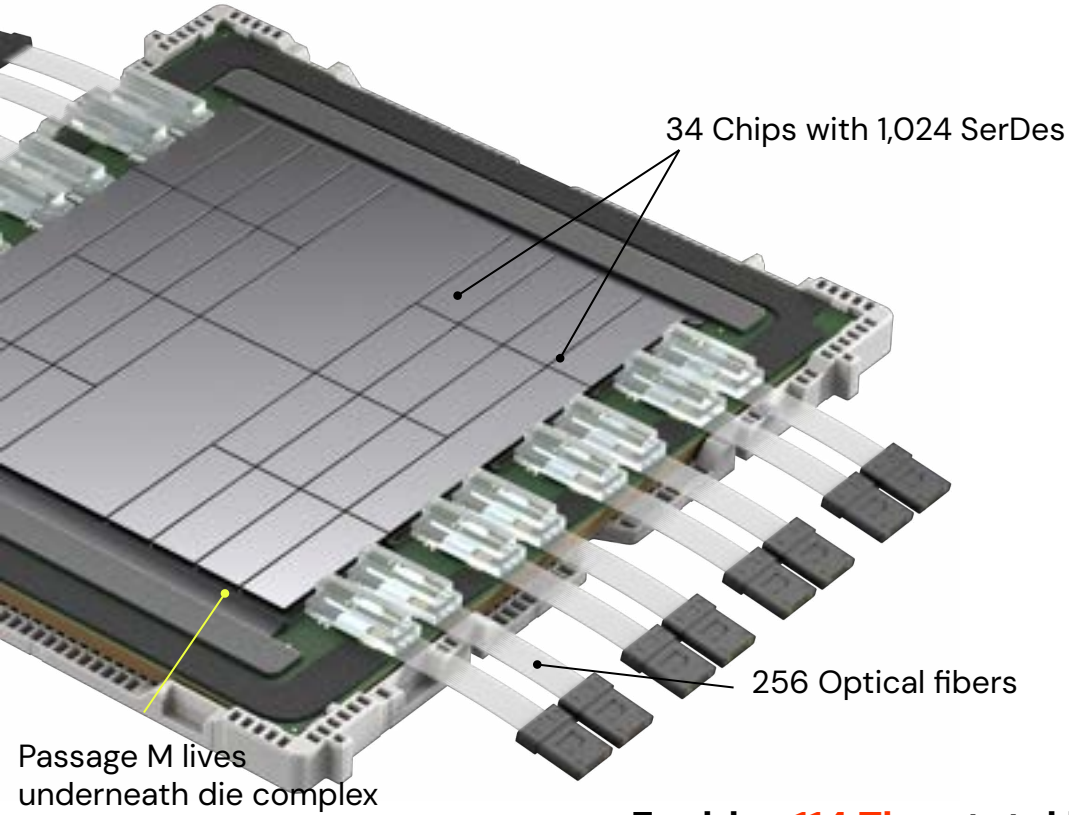
Passage™ M Series: Multi-Reticle PIC



LIGHTMATTER

Passage™ M Series

Photonic interposer reference platform

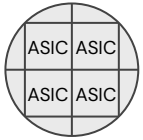


Specifications	
Bandwidth (Tx + Rx)	Up to 114 Tbps
# of SerDes	1024
Silicon die Complex	4,000 mm^2
Power delivery	>1.4 W/mm^2 density
Fibers	256
Redundancy	Optical circuit switching
Substrate Form Factor	91x85mm

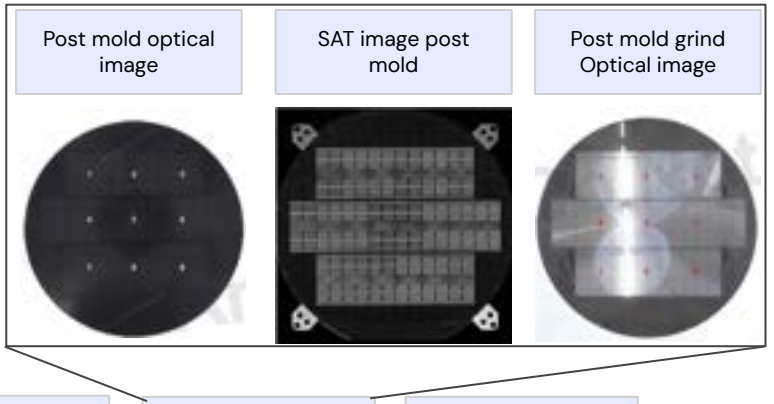
Enables 114 Tbps total bandwidth.

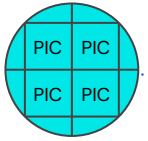
LIGHTMATTER

M1000 How it's built.



ASIC





Wafer Test

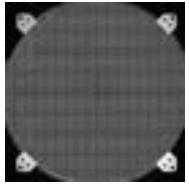
TSV Reveal

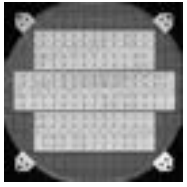
RDL and bumping

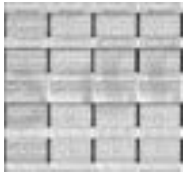
CoW reflow: PIC wafer (TSV) to ASIC attach

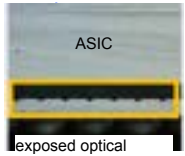
Wafer level underfill, mold and grind

Wafer dicing









exposed optical waveguide in the PIC

System

Final electro-optical test

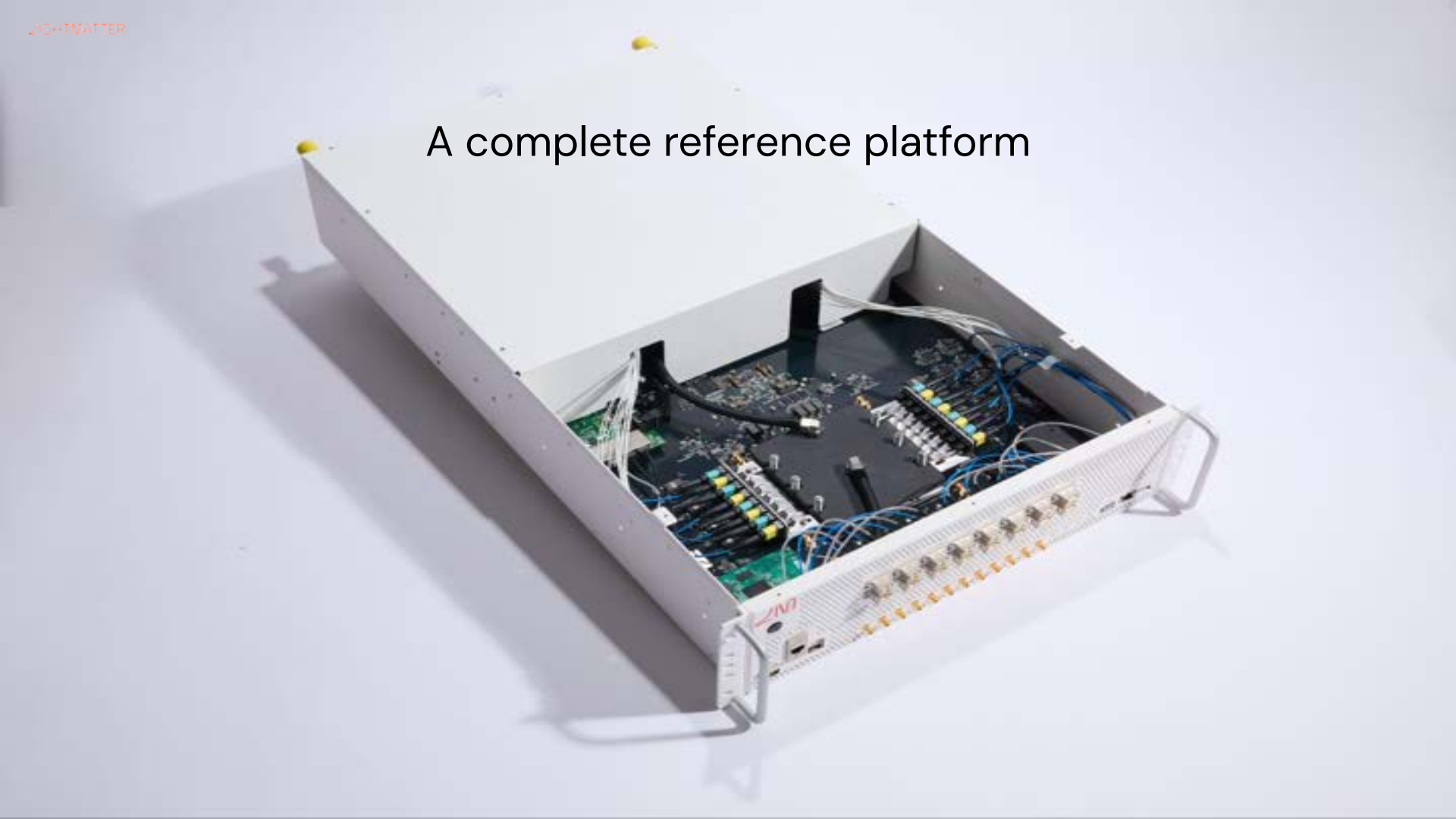
Fiber attach with real time optical test

Package e-test (Known good PKG)

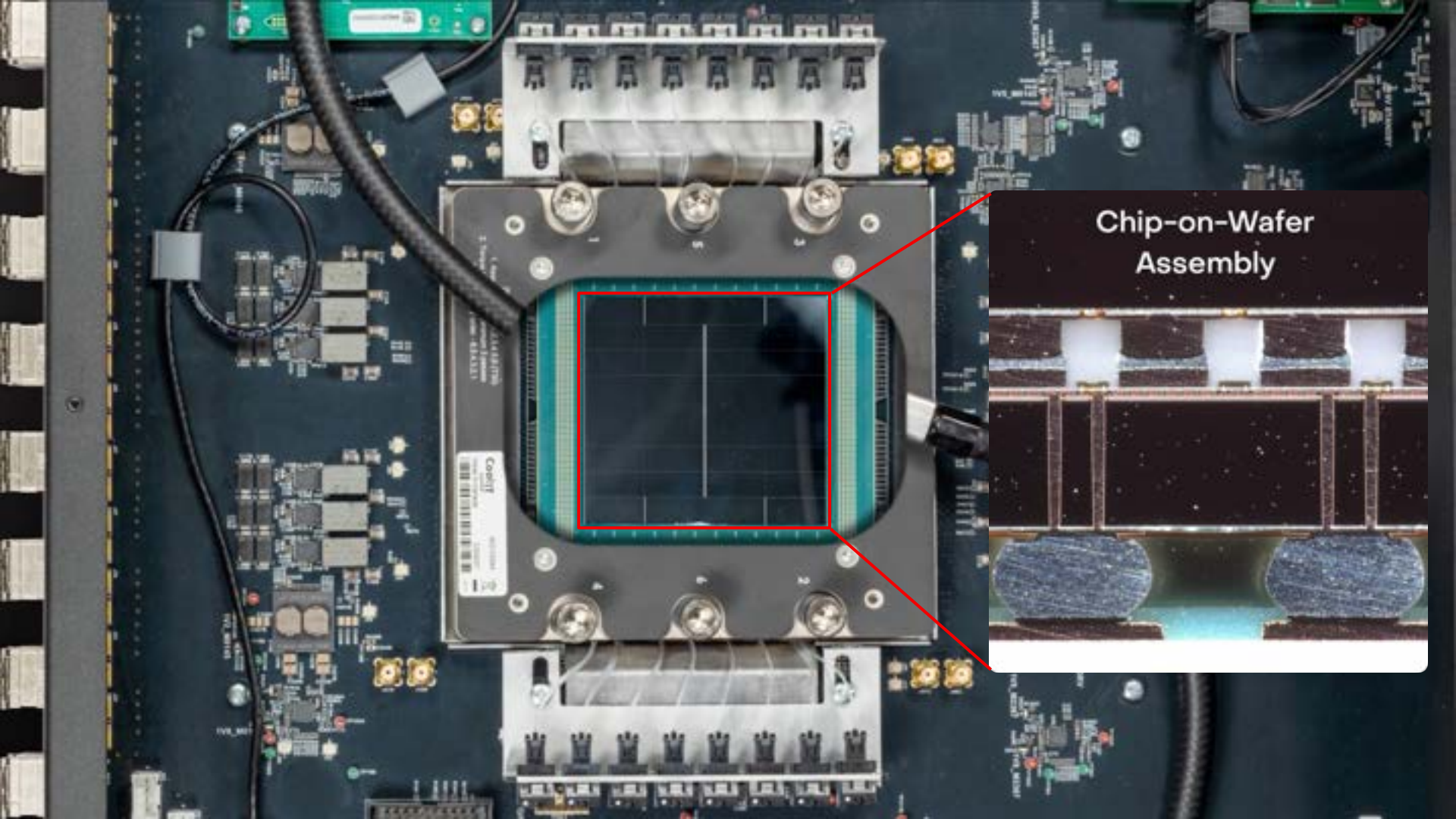
Heat sink attach

Post substrate attach reflow

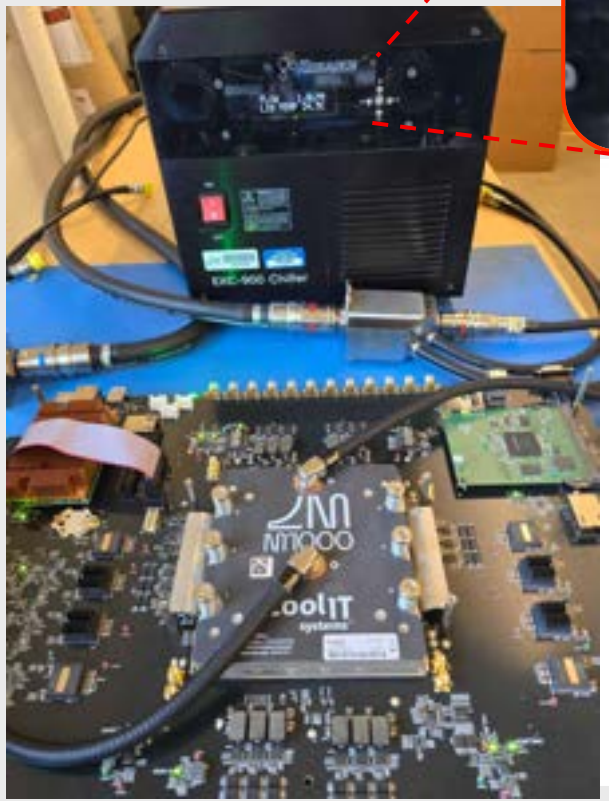
A complete reference platform

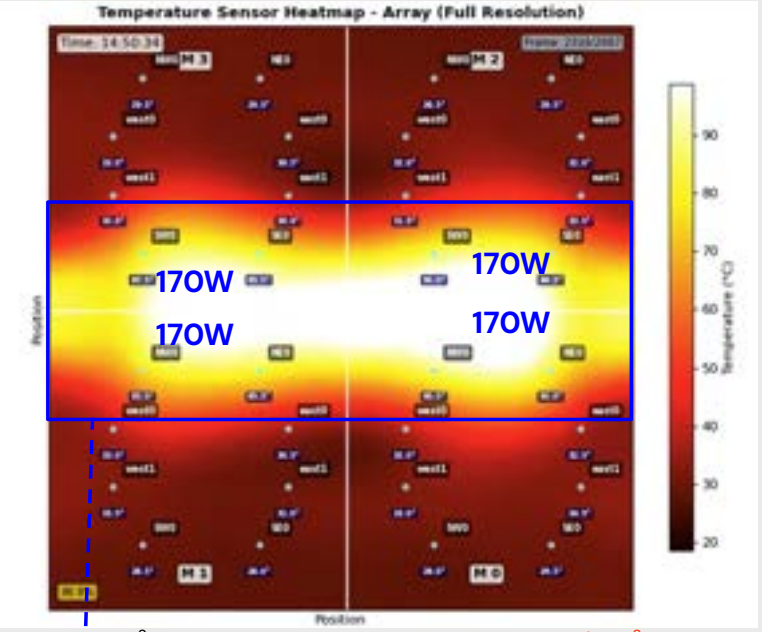



M1000
CoolIT
systems


Chip-on-Wafer
Assembly

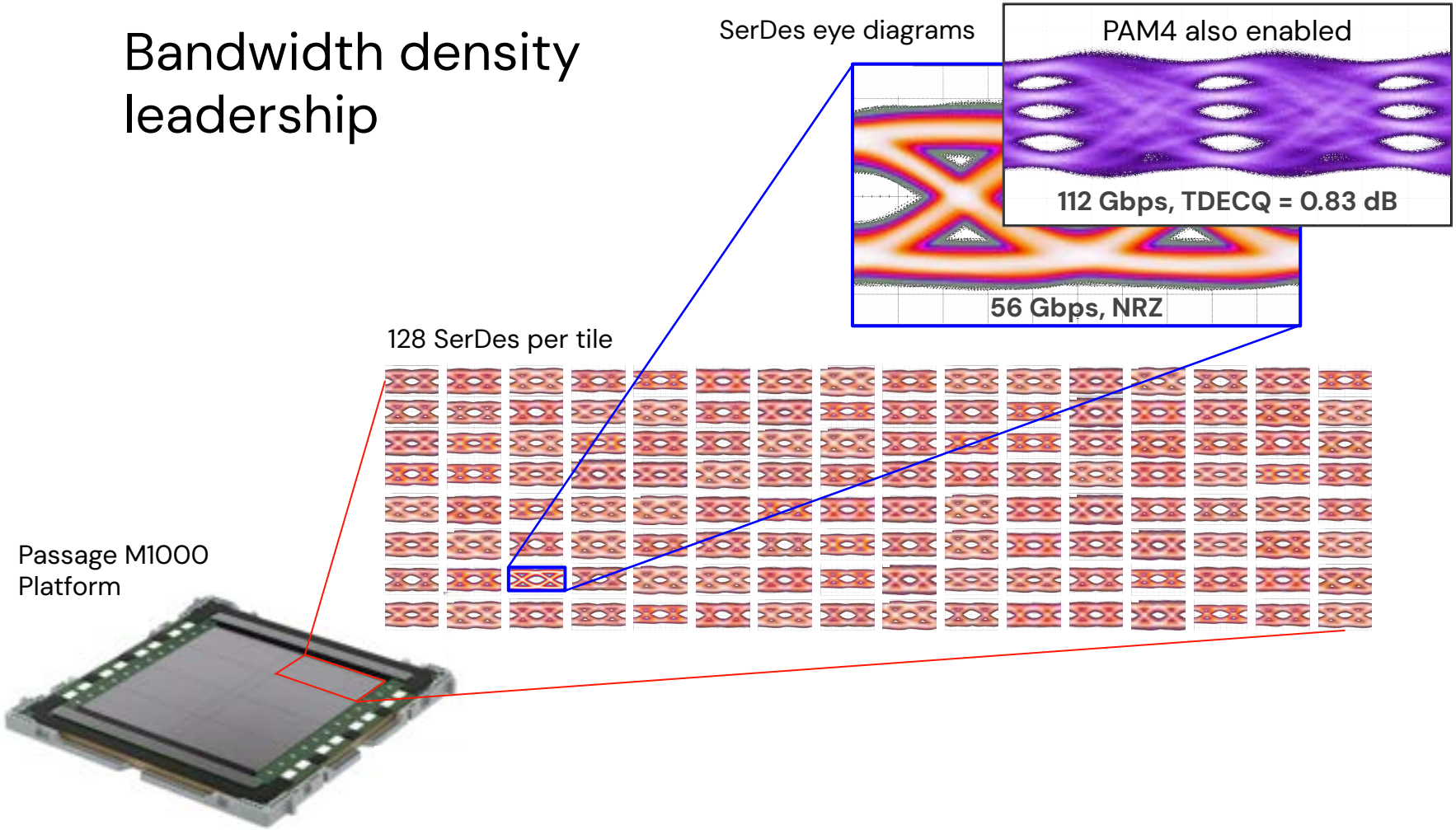
Power delivery and thermal load





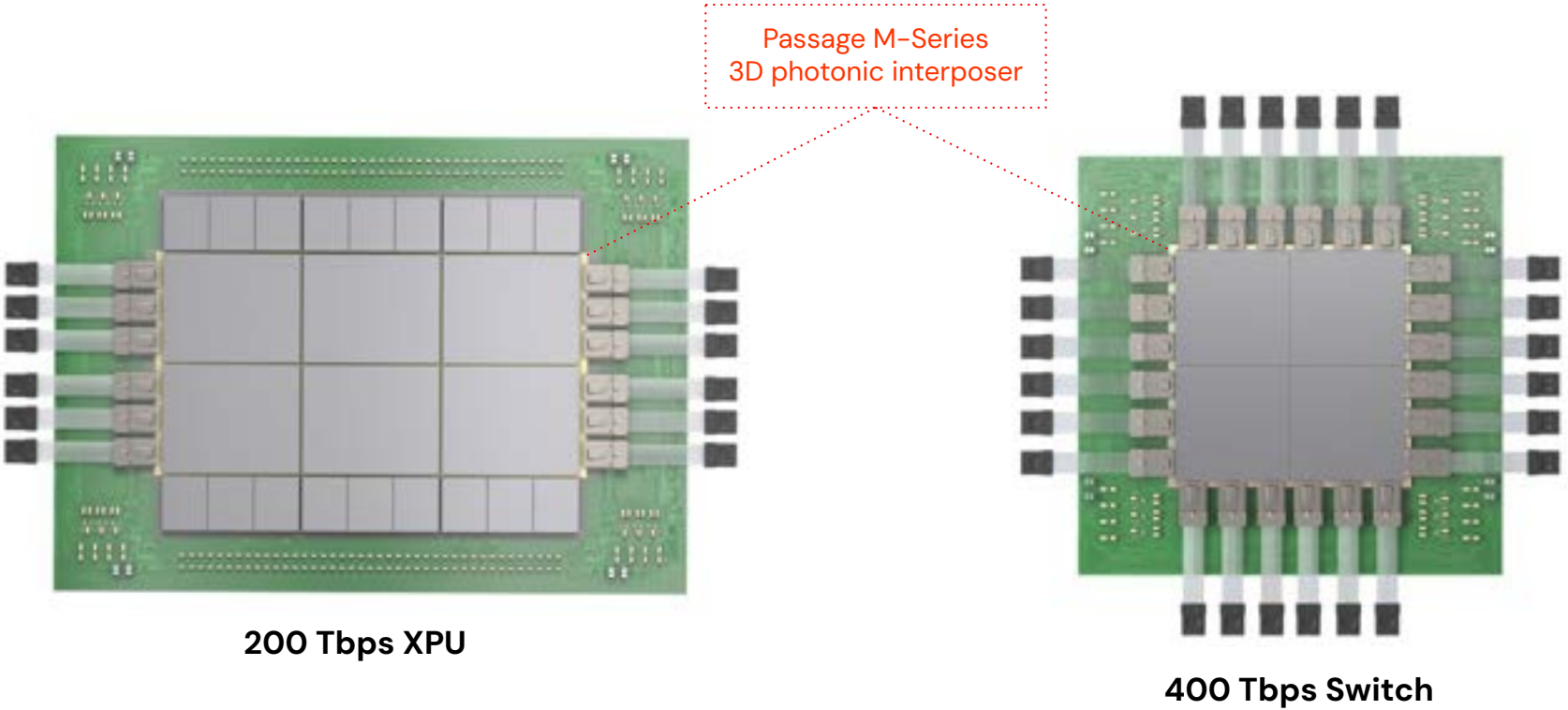
369mm^2 thermal test chip, power density 1.47W/mm^2.
Passage TSVs support >2.5A/mm^2.

Bandwidth density leadership



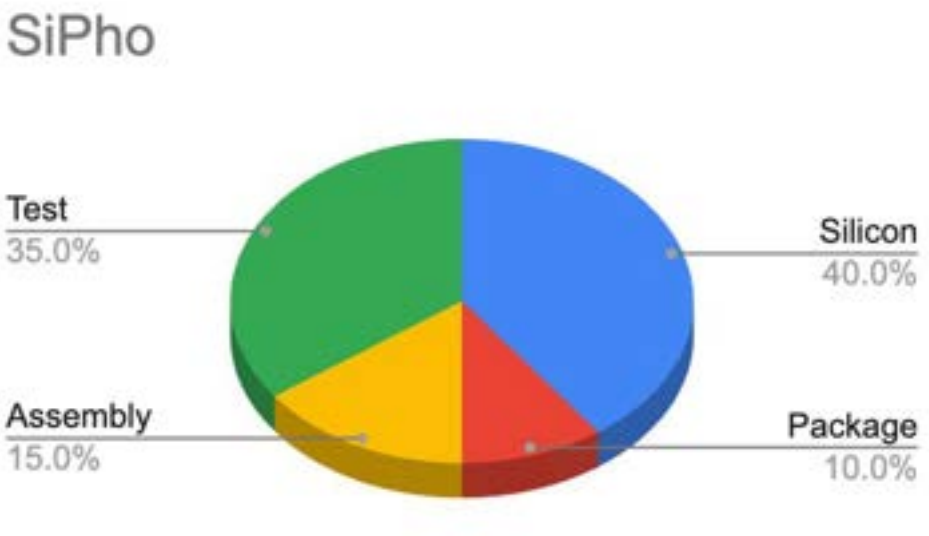
3D Interposer scale-up and out to 1M nodes

The M1000 revolution



SPAT Costs and the Need for continued Innovation

Silicon, Package, Assembly, Test



Note: Graph shown for demonstration purposes only

For SiPho Relative Packaging, Assembly and Test (PAT) cost % is increasing

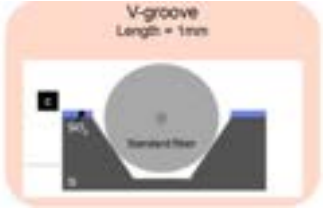
PAT cost challenges in SiPho:

1. In assembly: fiber attach yields
2. In test: test times are much higher

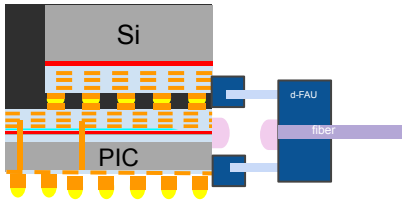
DFM/DFT-driven product architecture is must for high volume SiPho manufacturing and cost reduction

Fiber Attach Methods

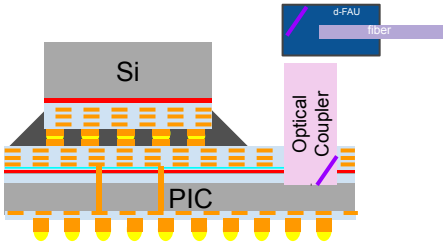
Traditional FAU



Lens based edge attach



Wafer Level Optical coupler



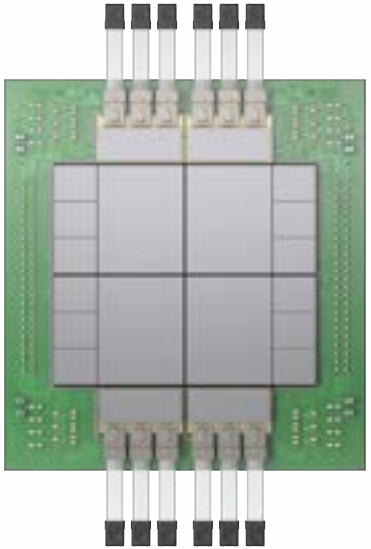
V-Groove based Fiber Attach Methods	**Lens based: Detachable fiber attach**	**LM Focus: Detachable fiber attach**
Package level assembly (interface on die edge)	Package level assembly (interface on die edge)	Wafer level assembly and test compatible
Not compatible with 3D Arch	**Compatible with 3D Package Arch**	**Compatible with 3D Package Arch**
XPU to OE D2D: Standard Package	**XPU to OE D2D: Standard & Adv. Package**	**XPU to OE D2D: Standard & Adv. Package**
Passive or Active alignment	Active alignment	Passive or Active alignment
Test with FAU after package assembly	Test with FAU after package assembly	Test with FAU at wafer level
FAB: GF only	FAB: GF & TSMC	FAB: GF & TSMC
Serviceability: No	**Serviceability: Yes**	**Serviceability: Yes**
Limited scalability to HVM ($$$)	Scalability to HVM ($$)	HVM scalable solution ($)

LM driving strong ecosystem partnership to bring detachable FAUs to HVM scale

Optimized end-to-end and production-ready

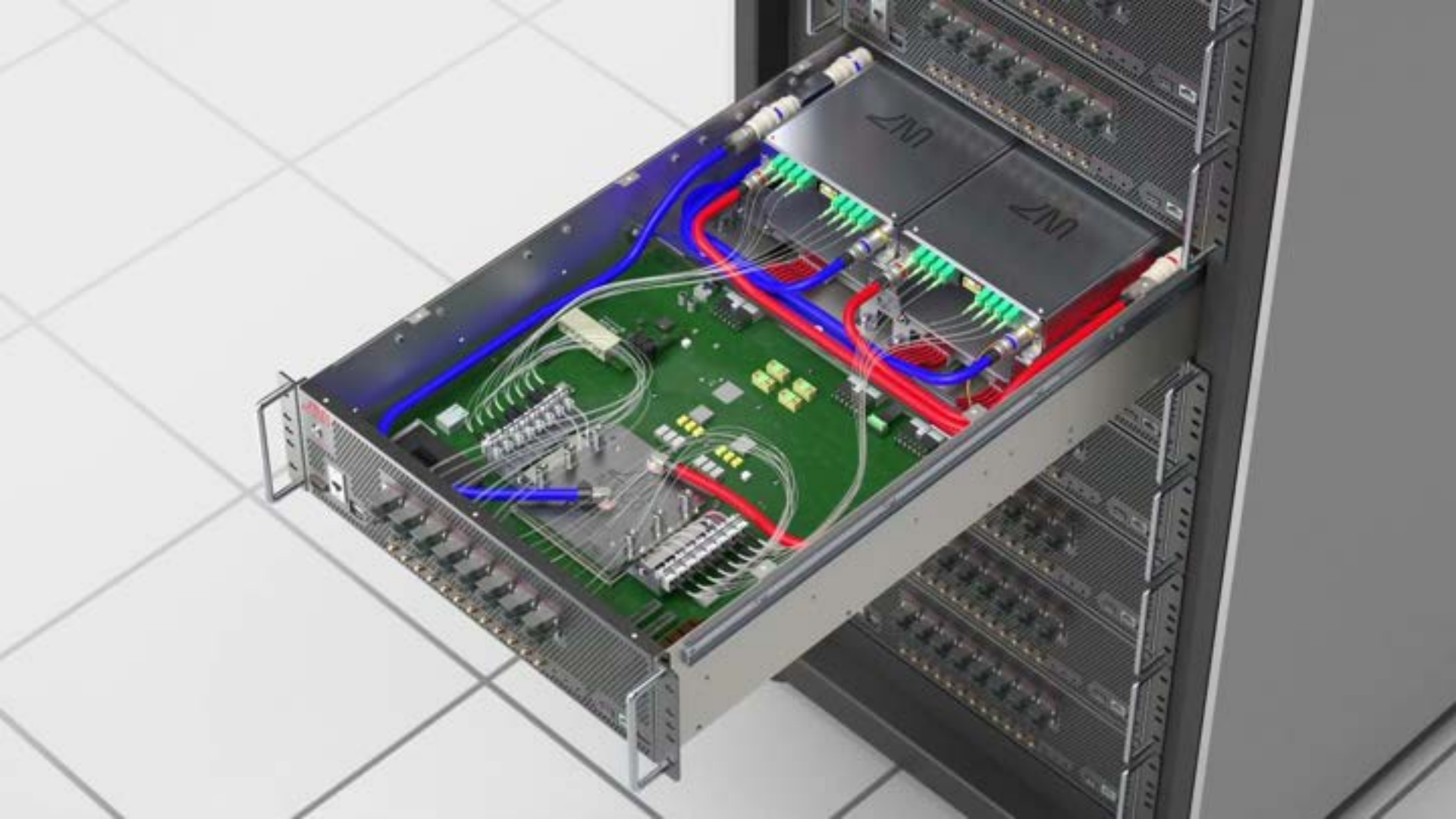
Customer ASIC with UCIe IP	**Multiple fabs**
Passage EIC	tsmc
LIGHTMATTER Passage PIC	tsmc / Tower
Pluggable fiber coupler	**Strategic partner**

tsmc
ASE
Amkor Technology



Laser module

16λ, 100 mW/fiber



THANK YOU