Monolithically Integrated Microring Transmitter and Receiver for High-Density 3D Co-Packaged Optics

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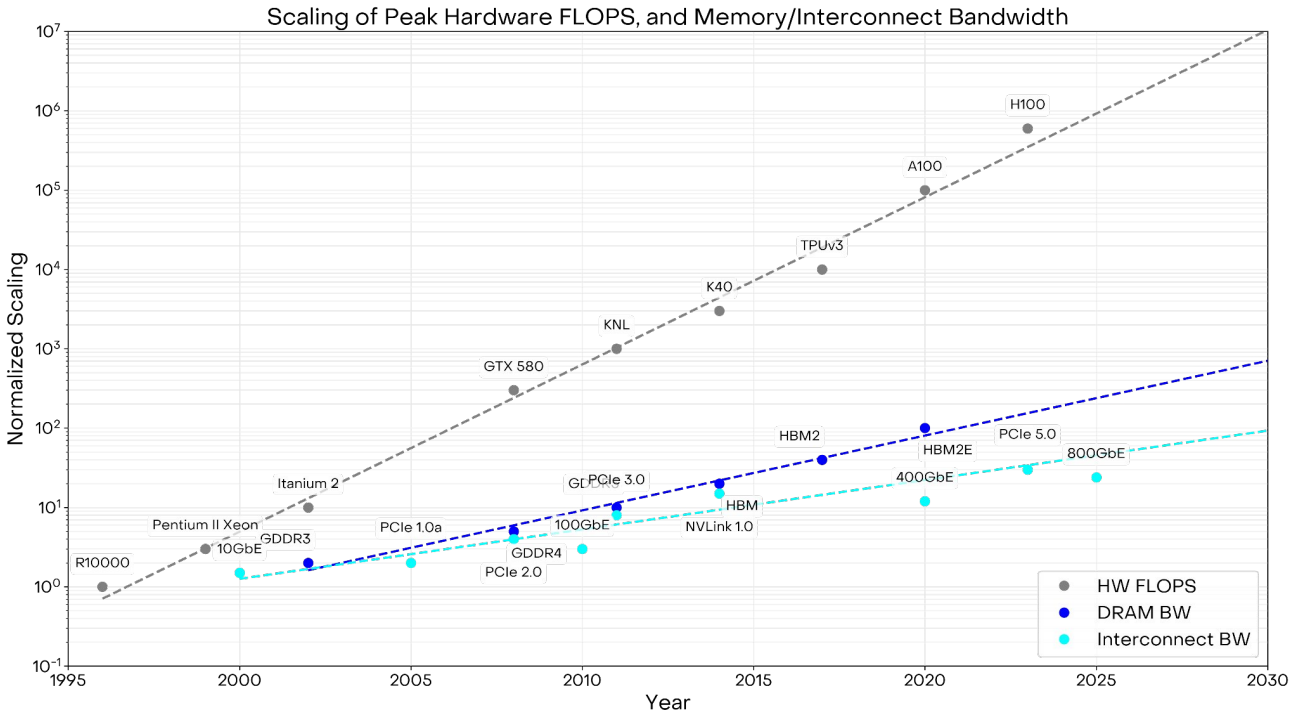
Solving the Biggest Bottleneck in AI Data Centers

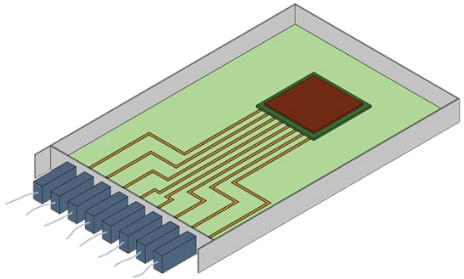
Interconnect bandwidth



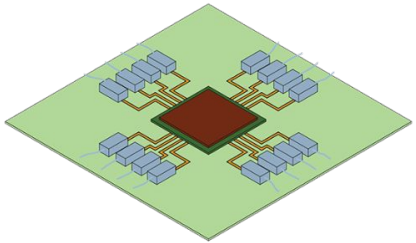
Gholami A, Yao Z, Kim S, Mahoney MW, Keutzer K. AI and Memory Wall. RiseLab Medium Blog Post, University of California Berkeley, 2021, March 29.

Enabling interconnects

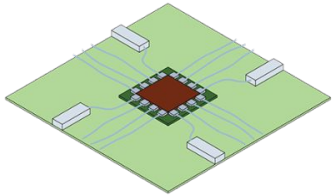
Gen I
Pluggable Optics



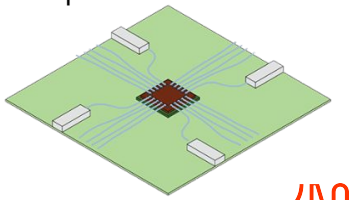
Gen II
On-board Optics



Gen III
2.5D Co-packaged Optics



Gen IV
3D Stacked Co-packaged Optics



Optical Links
Electrical Links
Pluggable Optical Transceiver

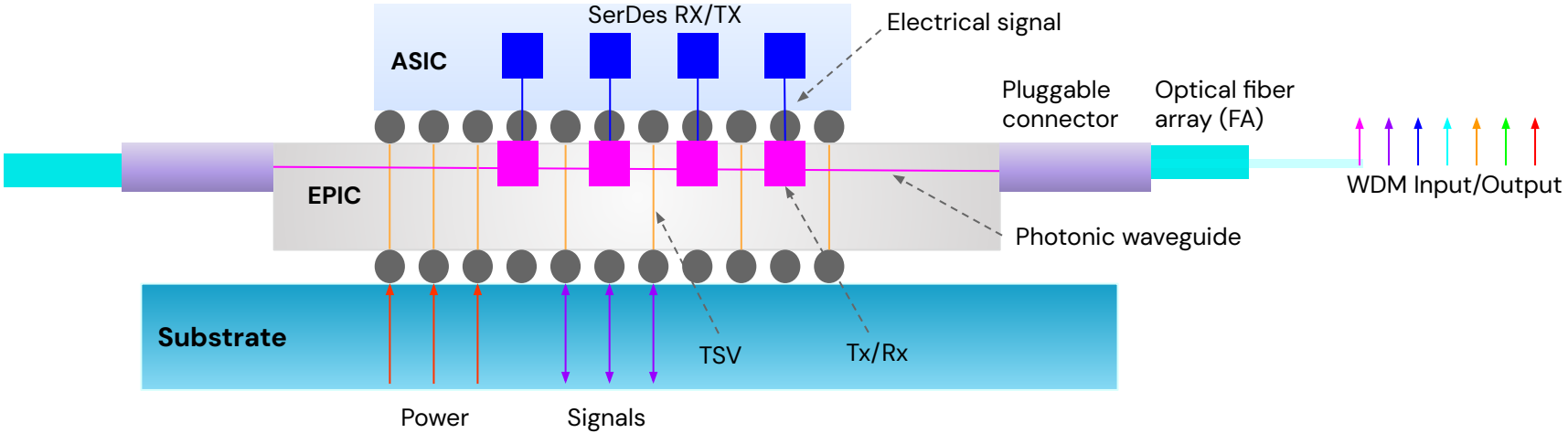
On-board Optics Module
Disaggregated Laser Supply
Co-packaged PIC

Why bring optics closer to the SoC?

- Reduction in interconnect power
- Increased bandwidth
- Higher bandwidth density at die edge
- Bypass intermediate stages (PCIe)

*Used with permission from Dr. John Bowers and adapted from an article in Applied Physics Letters (2021)

3D co-packaged optics requires compact modulators and receivers



Bump pitch: 120 μm
Bump size: 80 μm
Available area for electronics and photonics: 0.0144 mm²

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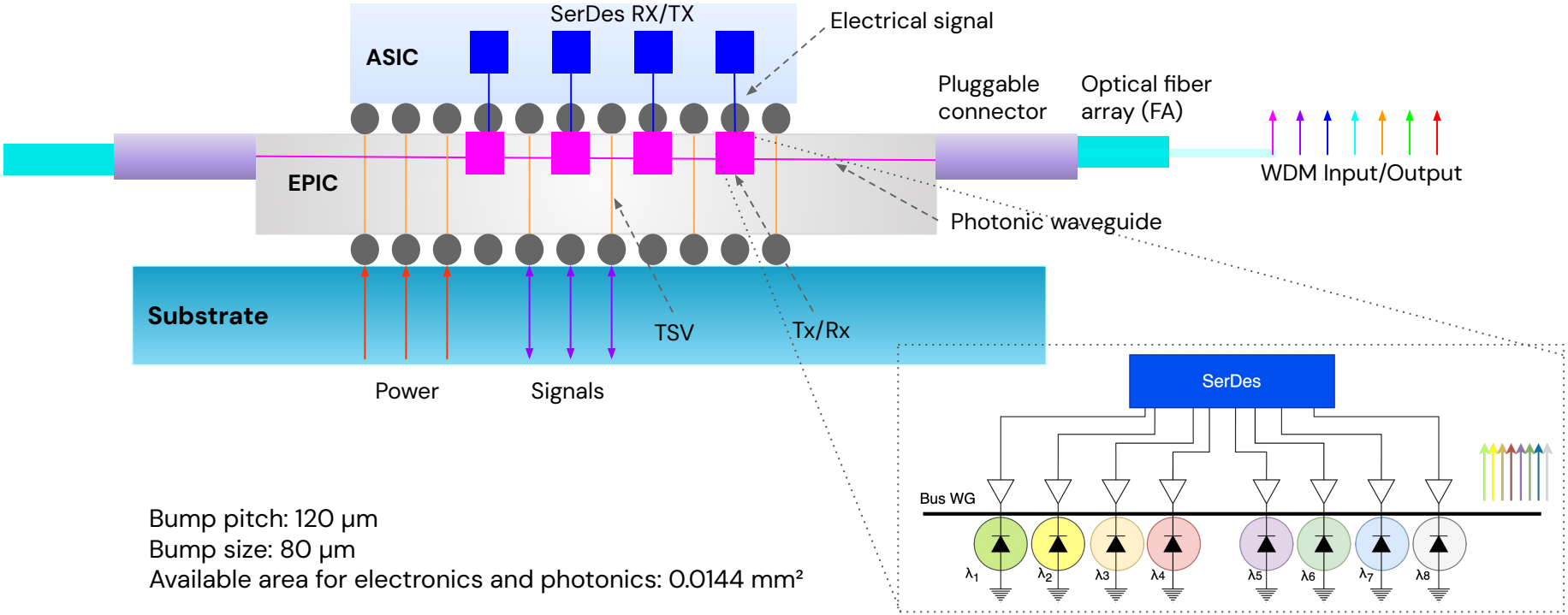

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State-of-the-art microring TX or RX for CPO

Parameter	Bhargava et al., 2024 (Ayar)	Schulien, 2022 (Ranovus)	Raj et al., 2023 (AMD)	Levy et al., 2024 (Intel)	Li et al., 2021 (Intel)
Data format	32 Gbps NRZ	106 Gbps PAM4	50 Gbps NRZ	50 Gbps NRZ	112 Gbps PAM4
Baud rate (Gbd)	32	53	50	50	56
Demonstration	TX + RX	TX + RX	RX	TX	TX
Integration	Monolithic	Monolithic	3D	3D	3D
CMOS node	45nm	45nm	7nm	28nm	28nm
Die Area (mm^2)	Not reported	Not reported	>0.031 active electronics	>0.025 active electronics	>0.4 active electronics
Bit-rate density (Tb/mm^2)	Not reported	Not reported	1.61	0.2	0.28
Efficiency (pJ/b)	3.45	2.75-3.1	0.96	2.5 incl. SerDes	6 incl. SerDes

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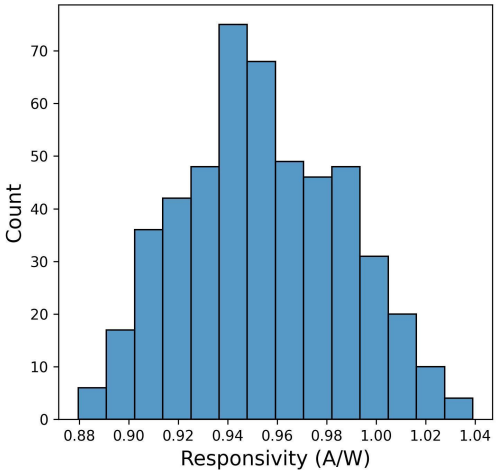
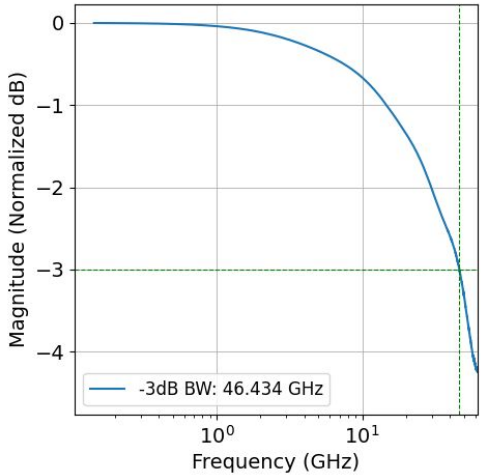
Optical RX: Micro Ring Resonator + PD

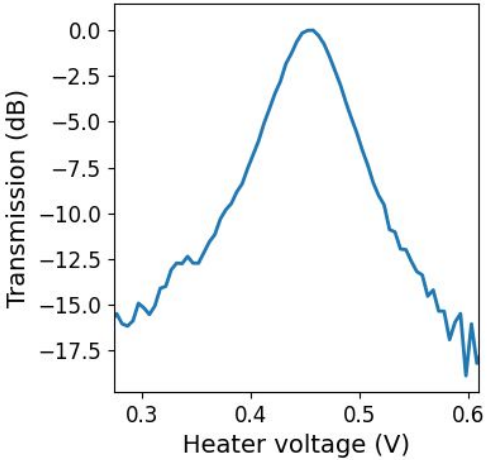
Responsivity Histogram



Measured OE BW

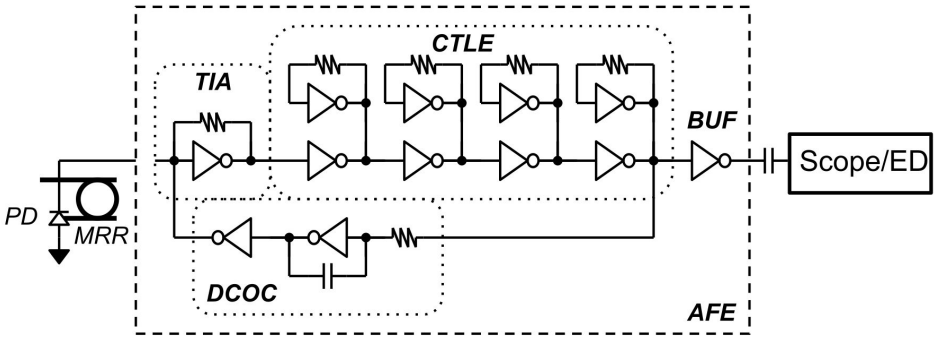


MRR detuning



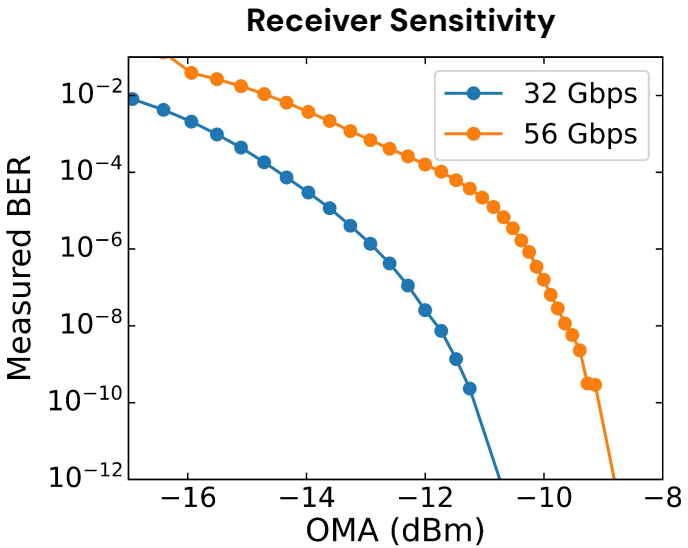
Parameter	MRR IL (dB)	MRR detuning efficiency	PD EO bandwidth	PD responsivity
Value	0.1 dB	>1.2FSR at 1.5 V	> 46 GHz	> 0.9 A/W

Receiver Architecture



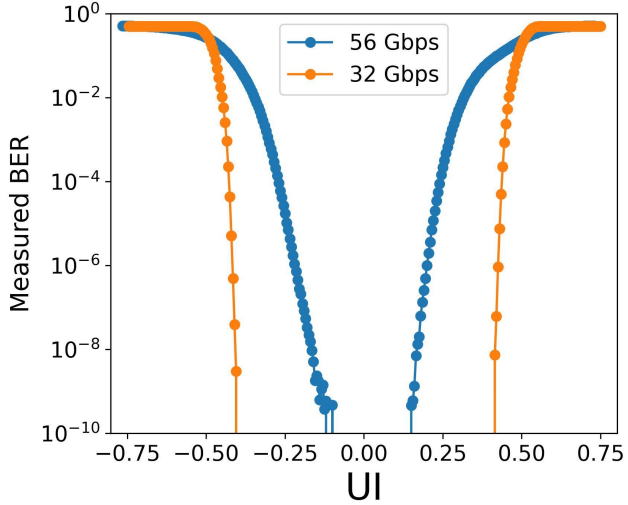
- Monolithically integrated MRR + Ge PD and analog front-end (AFE)
- AFE: TIA, CTLE, and DCOC
- 18 GHz bandwidth, 86 dBΩ gain, 400 mVpp output.
- Inductorless
- Compact footprint of 3.2×10^{-3} mm².

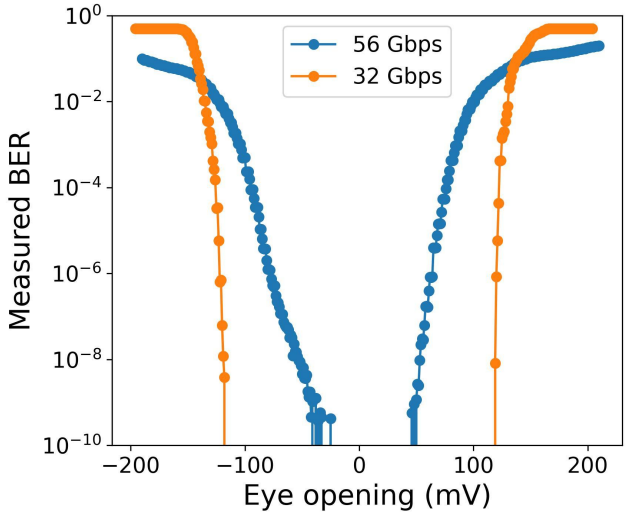
BER Measurements at 32G and 56G



	Min. received OMA
32 Gbps NRZ, PRBS9, BER < 10^{-12}	-11 dBm
56 Gbps NRZ, PRBS9, BER < 10^{-12} (with FFE (4 taps) on BERT)	-9 dBm

BER Bathtub Measurements at 32G and 56G





Settings:

- 32Gbps with no equalization
- 56Gbps has FFE (4 taps) equalization
- PRBS9
- No degradation at PRBS15

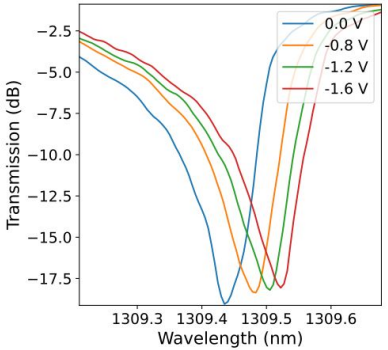
Optical TX: Micro Ring Modulator

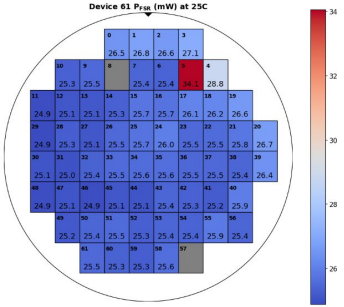
Parameter	Tuning efficiency	EO bandwidth	Quality factor
Value	50 pm/V	> 30 GHz	3500

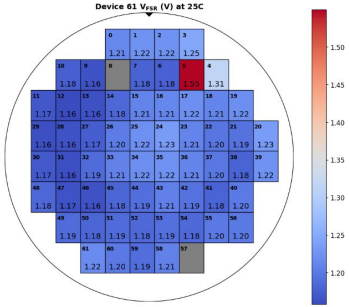
- Bias for max OMA
- Wafer-scale characterization

Data from many wafers and lots

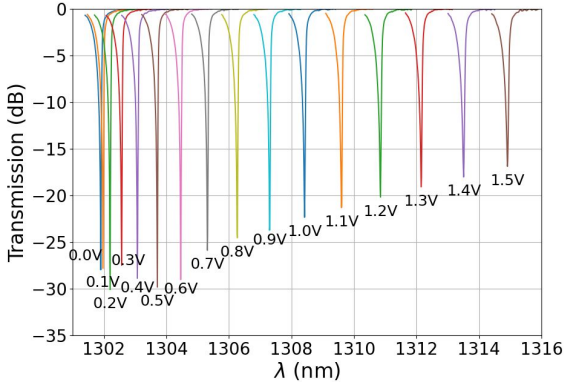
PN junction bias wavelength detuning



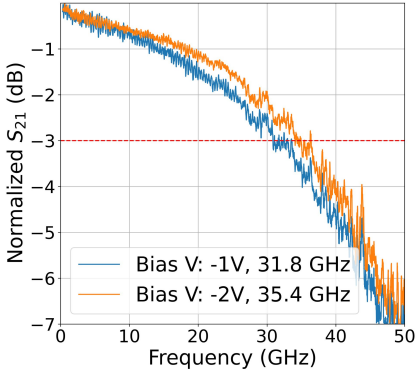




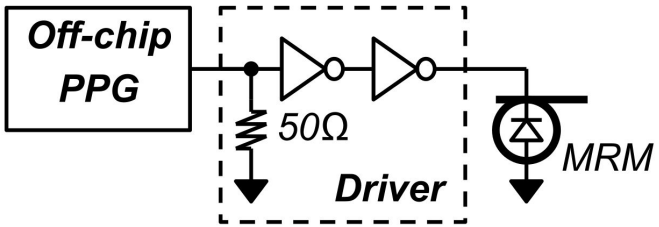
Thermal wavelength detuning



Measured EO S21



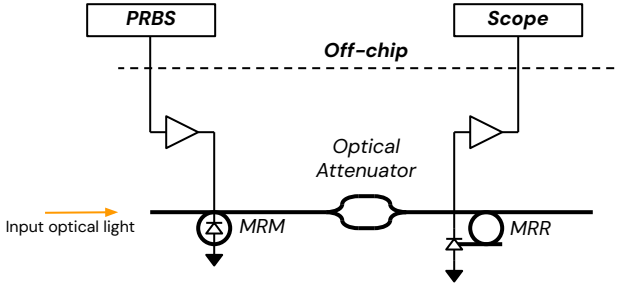
Transmitter Architecture

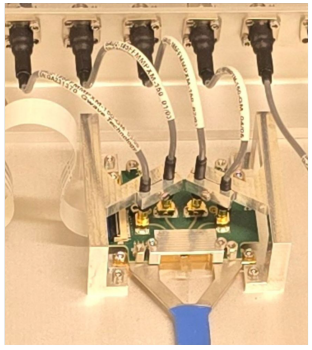


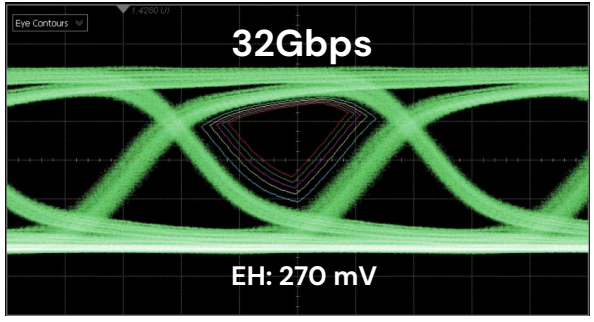
- Monolithically integrated driver and MRM in 45nm CMOS
- Driver Details:
  - **Inductorless** Single-ended CMOS inverter with 50Ω input termination
  - Two-stage buffer chain
  - Output swing: 1.3V pp (56Gbps)
- TX Die Area: 2.8×10^{-3} mm²

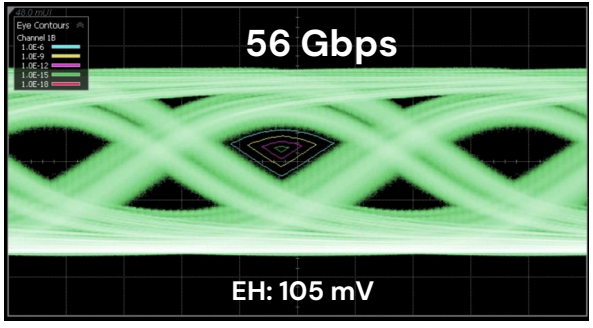
TX + RX characterization

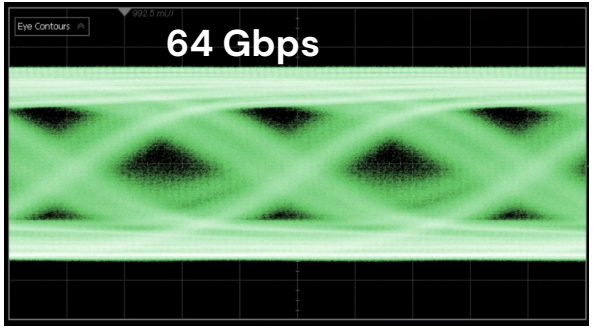
- Back-to-back TX and RX on the same chip
- TX + RX area: 0.006 mm²

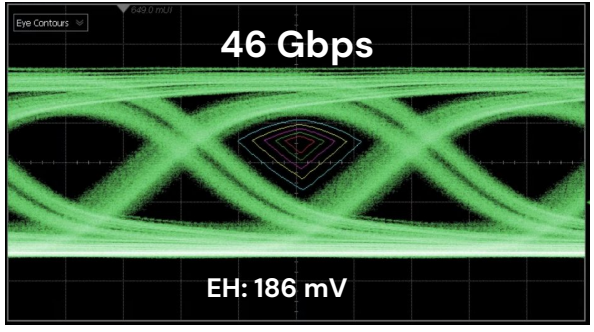


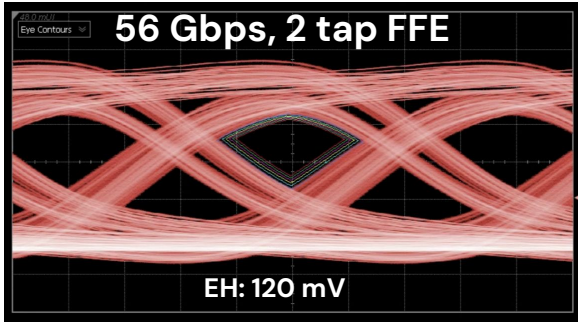


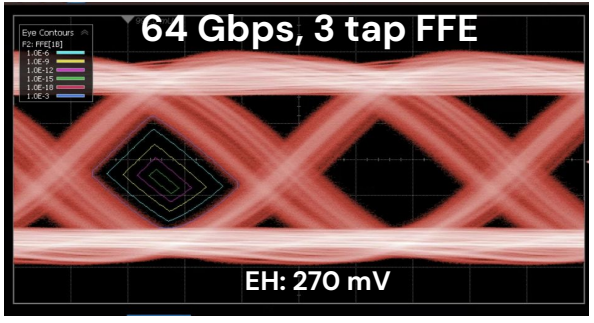












Comparison with State-of-the-Art

Parameter	This work	Bhargava et al., 2024 (Ayar)	Schulien, 2022 (Ranovus)	Raj et al., 2023 (AMD)	Levy et al., 2024 (Intel)	Li et al., 2021 (Intel)
Data format	56 Gbps NRZ	32 Gbps NRZ	106 Gbps PAM4	50 Gbps NRZ	50 Gbps NRZ	112 Gbps PAM4
Baud rate (Gbd)	56	32	53	50	50	56
Demonstration	TX + RX	TX + RX	TX + RX	RX	TX	TX
Integration	Monolithic	Monolithic	Monolithic	3D	3D	3D
CMOS node	45nm	45nm	45nm	7nm	28nm	28nm
Die Area (mm^2)	**TX: 0.0028** **RX: 0.0032**	Not reported	Not reported	>0.031 active electronics	>0.025 active electronics	>0.4 active electronics
Bit-rate density (Tb/mm^2)	**10.7**	Not reported	Not reported	1.61	0.2	0.28
Efficiency (pJ/b)	**1.51**	3.45	2.75-3.1	0.96	2.5 incl. SerDes	6 incl. SerDes

Conclusions

AI hardware drives demand for optical solutions inside ASIC packages

3D copackaged optics requires compact (<0.0144 mm²) and energy-efficient optical transmitters and receivers

Key Achievements:

Ultracompact TX and RX (0.006 mm²) due to inductorless driver and AFE

56 Gbps operation, receiver sensitivity -9 dBm OMA

TX + RX energy efficiency: 1.5 pJ/bit

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