Monolithically Integrated Microring Transmitter and Receiver for High-Density 3D Co-Packaged Optics

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Abstract: We report silicon microring transmitter and receiver with monolithically integrated driver and analog front end at up to 64Gbps NRZ. The total die area of the circuits is 0.006 mm^2, >10x smaller than prior reports. © 2024 The Author(s)

1. Introduction

The rapid growth of AI demands computing systems with not only unprecedented processing capabilities but also unparalleled communication bandwidth. As AI supercomputers scale up, advanced interconnect solutions are crucial to handle the massive data communication between the processing units (XPUs) and/or switches. Traditional electronic interconnect solutions, with their limited range, hinder the performance and scalability of AI workloads. Optical interconnects can offer advantages in energy efficiency, sensitivity, density, bandwidth, and latency. Optical transceivers can be co-packaged with XPUs and/or switches using 2.5D or 3D packaging approaches. 2.5D co-packaged optics (CPO) is ultimately limited by the beachfront density between the XPU and optical transceivers. A 3D CPO solution (Fig. 1(a)), where the photonics are effectively contained in an interposer under the XPU, demands photonic components as well as their drivers and analog front ends (AFEs) be as compact as possible and monolithically integrated. This reduces the area contention in the XPU where precious real estate in a leading-edge CMOS node could have been used for computation.

Silicon photonics (SiPh) technology can offer the monolithic integration of photonic circuits and CMOS. Monolithically integrated optical transmitters (Tx's) and receivers (Rx's) have been demonstrated in SiGe BiCMOS up to 56 Gbps NRZ [1, 2] and in CMOS SiPh up to 112 Gbps PAM4 [3, 4, 5, 6]. Both Mach-Zehnder modulator (MZM) and microring modulator (MRM) architectures have been demonstrated. However, MZMs are millimeter-long while the compact footprint of MRMs are better matched to the IO density of a 3D package. Moreover, a set of bus-waveguide coupled resonators supports wavelength division multiplexing (WDM) without additional devices. A challenge in maintaining a compact Tx and Rx footprint is the passive inductors in CMOS, which are ~0.1 mm^2-sized and commonly used for inductive peaking for bandwidth extension [6].

Here, we present an ultracompact monolithic transceiver *without any passive inductors* in a 45nm CMOS SiPh process. The Tx consists of a MRM with its driver, and the Rx consists of a microring resonator (MRR) with a

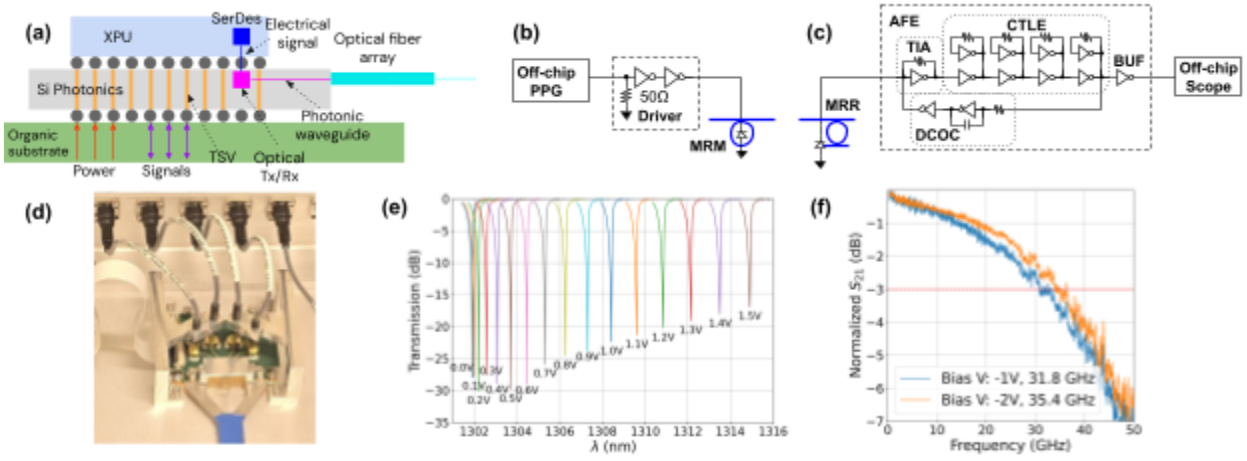

Fig. 1. (a) Schematic of 3D CPO. The bumps and through-silicon-vias due to the XPU-to-organic-substrate connectivity demands compact Tx and Rx in the Si photonic interposer. (b) Tx consisting of a driver and the MRM in blue, (c) Rx consisting of the AFE and MRR in blue, (d) Photograph of the packaged chip containing Tx and Rx for testing, (e) MRM spectra at different heater voltages. (f) MRM S_{21} response at two bias voltages showing a 3dB bandwidths near 34.1 GHz for a -2V bias.

56GHz-bandwidth germanium (Ge) photodetector (PD) at the drop port and the AFE (Fig. 1(b)-(d)). The Tx and Rx pair occupied an area of only 0.006 mm^2 on die and operated at up to a 64 Gbps NRZ. To the best of our knowledge, this is the densest—in terms of bit rate per die area ($Tbps/mm^2$)—monolithic microring Tx and Rx.

2. Design

To minimize the die area, we adopted a bus-waveguide coupled microring architecture for the inductor-less Tx and Rx as illustrated in Fig. 1(b) and (c). The MRMs and MRRs were designed for O-band operation with 1.8 THz FSR (compatible with 200 GHz spacing 8-λ WDM) and integrated heaters for wavelength tuning and stabilization.

The MRM was monolithically integrated with a single-ended inductorless CMOS inverter-based driver with 50Ω input termination. The two-stage buffer chain provides a CMOS rail-to-rail output swing equal to the supply voltage at the MRM optical output. The simulated output voltage swing is 1.3 Vpp at 56 Gb/s using a supply voltage of 1.3V. The MRM and driver occupy a die area of 2.8×10^{-3} mm^2.

In the MRR, the Ge PD was integrated with a single-ended CMOS inverter-based AFE consisting of a shunt-feedback transimpedance amplifier (TIA), gyrator-based continuous-time linear equalizer (CTLE), DC offset cancellation (DCOC) loop, and output buffer. Monolithic integration of the PD and TIA minimizes input capacitance, enabling use of higher feedback resistor values in the kΩ range to achieve low input referred current noise. The CTLE is composed of a 4-stage amplifier chain leveraging inverter-based gm/gm amplifiers to enhance linearity [7] and active inductors to extend the bandwidth with minimal footprint [8]. The DCOC loop cancels the average photocurrent from the optical link. The loop leverages self-biasing and the Miller effect to provide a low sub-MHz cutoff frequency with minimal footprint. The output buffer drives an external 50Ω load via an external DC blocking capacitor. The AFE has a simulated gain of 86 dBΩ, bandwidth of 16 GHz, input-referred current noise PSD of 6.4 pA/sqrtHz, output voltage swing of 400 mVpp and eye height of 100 mVpp for a 20 μApp input with 80 μA average photocurrent at 56 Gb/s using a supply voltage of 1.3V. The MRR and AFE occupy a die area of 3.2×10^{-3} mm^2.

3. Measurement Results

3.1 Optical and S-parameter characterization

The designs were fabricated in the GF 45SPCLO platform. Fig. 1 shows our measurements of the MRM spectrum vs. applied bias voltage on the modulation junction. The MRMs have a voltage-dependent extinction ratio >18 dB (Fig. 1(e)). The integrated heaters provided tuning of 0.44 nm/mW. Figure 1(f) shows the S21 of the MRMs. For the electro-optic S21 measurement, the input wavelength to the MRM was tuned to maximize the S21 below the 3dB bandwidth, corresponding to the point of maximum modulation efficiency. The MRMs exhibited 3dB bandwidths in the range of 30.9 ± 2 GHz for a bias voltage of -1V. The PDs exhibited 3 dB bandwidth of 56 GHz at a bias voltage of -1 V.

3.2 Tx and Rx Characterization

A die containing the Tx and Rx was assembled onto a custom designed printed circuit board (PCB) and connected via short pitch-controlled wire bonds, to achieve minimal impedance mismatch. The PCB had 1.85mm SMP connectors, with tuned impedance connector launches, low loss dielectric, 50 ohm (SE) controlled impedance transmission lines; designed to facilitate 56Gbps (NRZ) high-speed testing. Fig. 1(d) shows a photograph of the assembly. The Tx and Rx were connected to each other via an on-chip waveguide. The input light from an off-chip

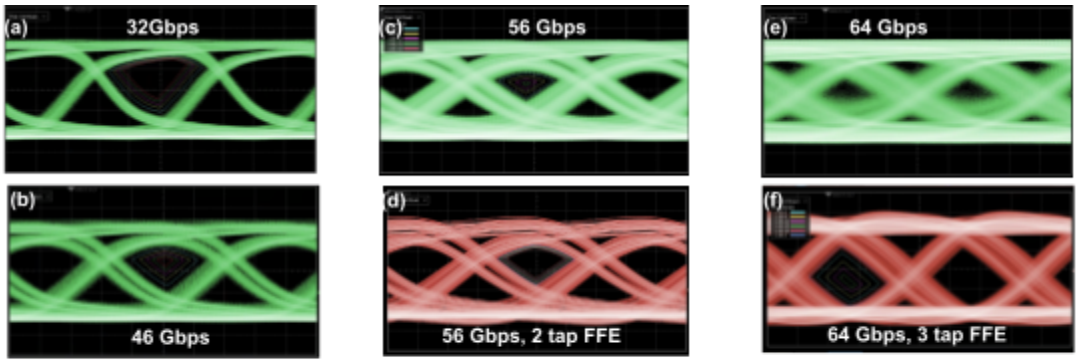

Fig. 2. Raw eye diagrams for data rates of (a) 32, (b) 46, (c) 56, and (e) 64 Gb/s at an average received optical power of -1.5 dBm. The eye amplitudes with software FFE at (d) 56 Gb/s (2 taps) and (f) 64 Gb/s (3 taps) increased the eye opening. The eye height values are described in the main text.

laser source was fiber-coupled to the MRM using a grating coupler via a fiber array attached to the die. Initialization and stabilization algorithms automatically locked the MRMs and MRRs to the input laser wavelength. A pulse pattern generator (PPG) provided pseudo-random binary sequence (PRBS) patterns with output swing of 0.9 Vpp. The output was connected to the PCB's SMP connectors via a 150 mm long coaxial cable. The measured electrical insertion loss between the PPG and the chip at the Nyquist frequency was about -6 dB. External power supplies provided the supply and DC bias voltages. The input optical power to the MRM was about 4 dBm, and the modulation insertion loss was approximately 4.9 dB.

Fig. 2(a)-(f) show the captured eye patterns at 32, 46, 56, and 64 Gbps using PRBS9 for an average received optical power of -1.5 dBm. The time-shifted rising and falling edges in the eye patterns may be due to reflections from the cable and PCB. Despite the degraded signal, the eye patterns were open at up to 56 Gbps without equalization. At 32 Gbps, the eye height was 270 mV with a bit error rate (BER) inferred using the Keysight FlexDCA N1000 series software on the sampling oscilloscope of $<10^{-18}$. At 46 Gbps, the eye height was reduced to 186 mV. At 56 Gbps, the eye height without equalization measured 105 mV. With a Rx 2-tap feed-forward equalization (FFE) at the Rx in software (Keysight FlexDCA) on the sampling oscilloscope, the eye height increased to 120 mV. At 64 Gbps, the raw eye pattern was starting to close, but Rx FFE with 3 taps boosted the eye height to 270 mV with an inferred BER on the sampling oscilloscope of $<10^{-12}$. Direct BER measurements using a BER tester were not possible due to instrumentation limitations, but measurement results will be presented at the conference.

4. Discussion

Table 1 compares our results with the single-wavelength performance of state-of-the-art microring Tx and Rx. Integration refers to how the driver and/or TIA were integrated with the microring. Density refers to the bit rate per area on the die. For 3D CPO, this metric is relevant for comparing maximum IO throughput for the XPU. For the demonstrations using 3D integration x[9, 10, 11], only the active die areas in the CMOS electronics (excluding any passive inductors) were reported. A microring occupies an area of the order of 10^{-3} mm^2 and does not dominate the area. Our Tx and Rx had a power consumption of 84.4 mW (excluding the laser), translating to an efficiency of 1.51 pJ/bit at 56 Gbps. Compared to prior microring Tx and Rx, this work shows the highest bit rate per area density by >10x while maintaining a high efficiency.

Table 1. Comparison of Single-Wavelength Performance of Microring Tx and Rx

Parameter	This Work	Ref. [4]	Ref. [5]	Ref. [9]	Ref. [10]	Ref. [11]
Format	NRZ	NRZ	PAM4	NRZ	NRZ	PAM4
Baud rate (G)	56*	32	53	50	50	56
Bit rate (Gbps)	56	32	106	50	50	112
Tx or Rx	Tx+Rx	Tx+Rx	Tx+Rx	Rx	Tx	Tx
Integration	Mono.	Mono.	Mono.	3D	3D	3D
CMOS node	45nm	45nm	45nm	7nm	28nm	28nm
Die area (mm^2)	Tx: 0.0028 Rx: 0.0032	NR	NR	>0.031†	>0.25†	>0.4†
Bit-rate/area (Tbps/mm^2)	10.7	NR	NR	1.61	0.2	0.28
Efficiency (pJ/bit)	1.51	3.45	2.75-3.1	0.96	2.5**	6**

Mono: Monolithic; NR: not reported; *open eye without equalization; **including SerDes; †Active electronics only

5. Conclusion

In summary, we have demonstrated the highest baud rate and the densest Tx and Rx designed for AI computing systems. The architecture without passive inductors operates at up to 56 Gbps without equalization and is the smallest Tx and Rx to date at 0.006 mm^2 total area—compatible with high-density 3D CPO solutions.

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